MPQ2451-AEC1

Industrial/Automotive-Grade 36V, 2MHz, 0.6A Step-Down Converter AEC-Q100 Qualified

The Future of Analog IC Technology

DESCRIPTION

The MPQ2451 is a high frequency, step-down, switching regulator with an integrated high-voltage high-side power MOSFET. It efficiently provides up to a 0.6A output with current-mode control for fast loop response.

The wide 3.3V-to-36V input range accommodates a variety of automotive step-down applications, and the 3μA shutdown-mode quiescent current allows use in battery-powered applications.

The MPQ2451 achieves high power-conversion efficiency over a wide load range by scaling down the switching frequency under light-load condition to reduce the switching and gate driving losses.

Frequency fold-back prevents inductor current runaway during start-up. Thermal shutdown provides reliable, fault-tolerant operation.

The MPQ2451 is available in a cost-effective SOT23-6L and QFN-6L packages.

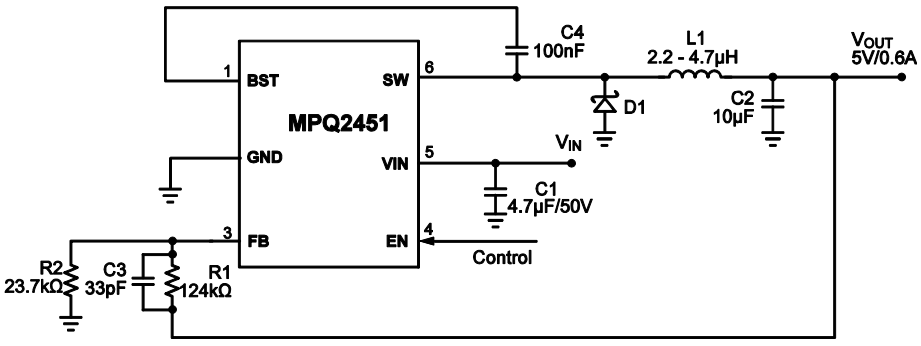
FEATURES

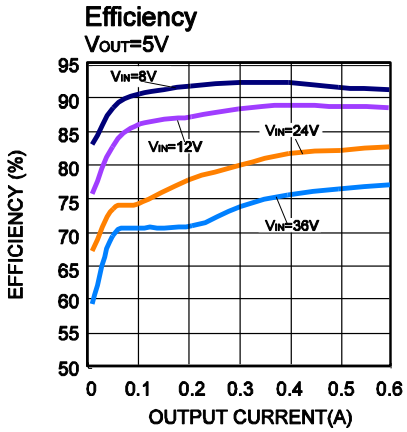
- Guaranteed Industrial/Automotive Temp. Range Limits
- 130μA Operating Quiescent Current
- Wide 3.3V-to-36V Operating Input Range
- 500mΩ Internal Power MOSFET
- 2MHz Fixed Switching Frequency
- Internally Compensated
- Stable with Ceramic Output Capacitors
- Internal Soft-Start
- Precision Current Limit Without Current Sensing Resistor
- >90% Efficiency
- Output Adjustable from 0.8V to 0.9·V_{IN}
- 6-Lead SOT23 and QFN Packages
- Available in AEC-Q100 Grade 1

APPLICATIONS

- High-Voltage Power Conversion
- Automotive Systems
- Industrial Power Systems
- Distributed Power Systems
- Battery-Powered Systems

TYPICAL APPLICATION





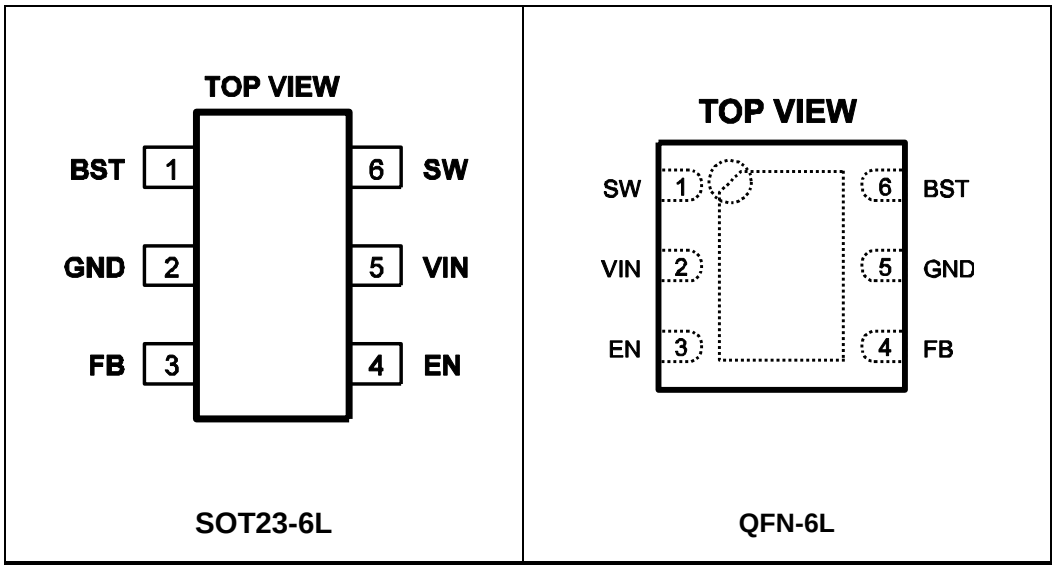
ORDERING INFORMATION

Part Number	Package	Top Marking	Junction Temperature (T_J)
MPQ2451DT*	SOT23-6L	V7	-40°C to +125°C
MPQ2451DT-AEC1	SOT23-6L	V7	-40°C to +125°C
MPQ2451DG**	QFN-6L	V7	-40°C to +125°C
MPQ2451DG-AEC1	QFN-6L	V7	-40°C to +125°C

* For Tape & Reel, add suffix –Z (e.g. MPQ2451DT–Z).
For RoHS Compliant packaging, add suffix –LF (e.g. MPQ2451DT–LF–Z)

** For Tape & Reel, add suffix -Z (e.g. MPQ2451DG-Z)
For RoHS Compliant packaging, add suffix -LF (e.g. MPQ2451DG-LF-Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage (V_{IN})..... -0.3V to +40V
Switch Voltage (V_{SW})..... -0.3V to (V_{IN}+0.3V)
BST to SW.....-0.3 to +5.0V
All Other Pins..... –0.3V to +5.0V
Continuous Power Dissipation (T_A = 25°C) (2)
SOT23-6L.....0.57W
QFN-6L.....1.56W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature.....-65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN}..... 3.3V to 36V
Output Voltage V_{OUT}.....0.8V to 0.9·VIN
Maximum Junction Temp. (T_J) .....+125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

SOT23-6L.....220 ....110 ..°C/W
QFN-6L.....80 .....16 ...°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J= -40°C to +125°C, unless otherwise noted. Typical values are at T_J = 25°C.

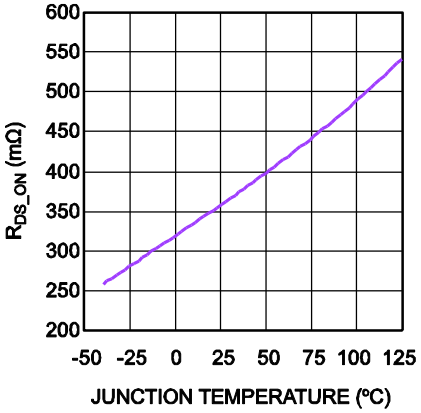
Parameter	Symbol	Condition	Min	Typ	Max	Units
Feedback Voltage	V_{FB}	4.0V < V_{IN} < 36V	0.774	0.794	0.814	V
		3.3V < V_{IN} < 4.0V	0.766	0.794	0.822	
Feedback Bias Current				0.05	1.0	µA
Upper Switch On Resistance	$R_{DS(ON)}$	V_{BST}-V_{SW}=5V T_J= 25°C		500		mΩ
Upper Switch Leakage		V_{EN} = 0V, V_{SW} = 0V		0.5	2	µA
Current Limit	I_{LIM}		0.65	1		A
COMP to Current Sense Transconductance	G_{CS}			3		A/V
V_{IN} UVLO Up Threshold			2.7		3.29	V
V_{IN} UVLO Hysteresis				0.4		V
Soft-Start Time		FB from 0 to 0.794V		0.5	1	ms
Oscillator Frequency	f_{SW}		1.4	2	2.6	MHz
Minimum Switch On Time	t_{ON}			100		ns
Shutdown Supply Current	I_S	V_{EN} < 0.3V		3	30	µA
Quiescent Supply Current	I_Q	No load, V_{FB}=0.9, no switching		130	200	µA
Thermal Shutdown				150		°C
Enable High Threshold	V_{IH}	Low-to-High	1.35	1.5	1.8	V
Enable Threshold Hysteresis				400		mV

PIN FUNCTIONS

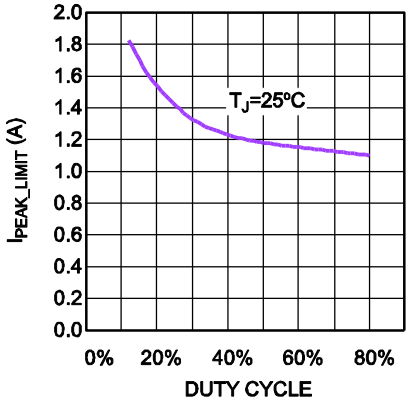
SOT23-6L Pin #	QFN-6L Pin #	Name	Description
1	6	BST	Bootstrap. Positive power supply for the internal floating high-side MOSFET driver. Connect a bypass capacitor between this pin and SW pin.
2	5	GND	Ground. Connect the output capacitor as close to this pin as possible. Avoid routing near high-current switch paths.
3	4	FB	Feedback. Input to the error amplifier. Connected to an external resistive divider between output and GND; compared against the internal 0.8V reference to set the regulation voltage.
4	3	EN	Enable Input. Pull this pin below the specified threshold to shut the chip down. Pull it above the specified threshold to enable the chip. Float this pin to disable the chip.
5	2	VIN	Input Supply. Supplies power to all internal control circuitry; both BS regulators and the high side switch. Requires a decoupling capacitor to ground close to this pin to reduce switching spikes.
6	1	SW	Switch Node. Output of the high-side switch. Requires a low V_F Schottky diode to ground close to this pin to reduce switching spikes.

TYPICAL CHARACTERISTICS

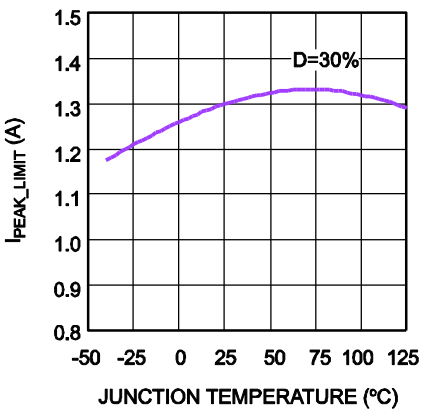
On Resistance vs. Junction Temperature



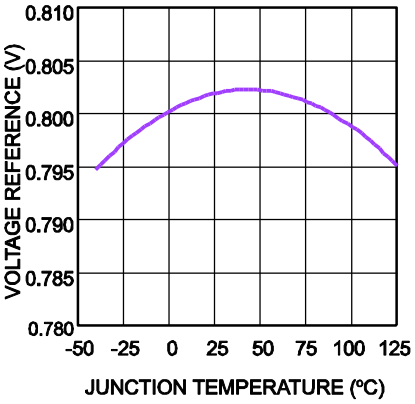
Current Limit vs. Duty Cycle



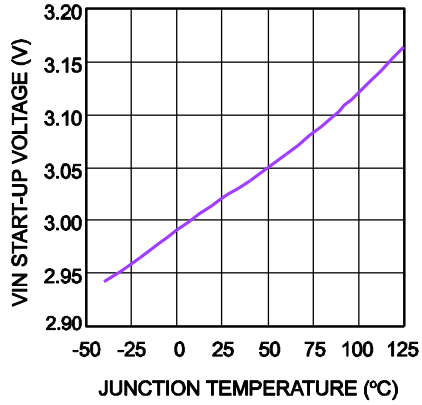
Current Limit vs. Junction Temperature



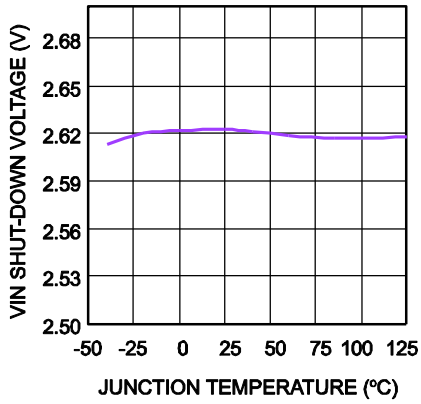
Voltage Reference vs. Junction Temperature



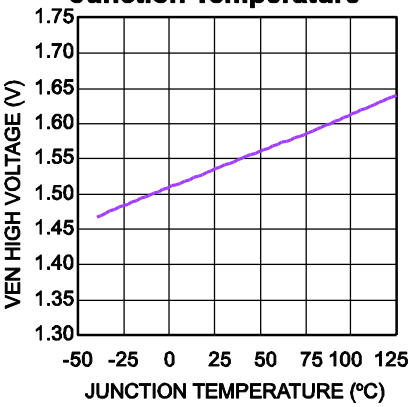
Vin Start-up vs. Junction Temperature



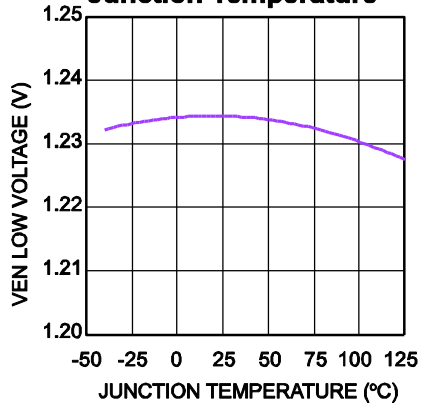
Vin Shut-down vs. Junction Temperature



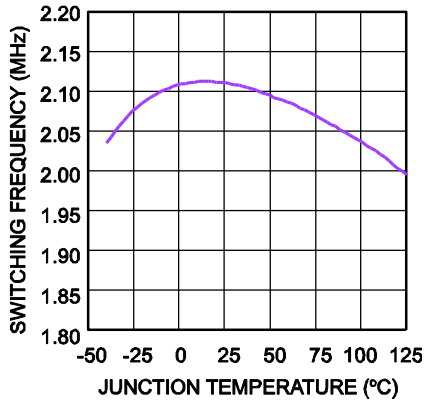
$V_{Enable-High}$ vs. Junction Temperature



$V_{Enable-Low}$ vs. Junction Temperature



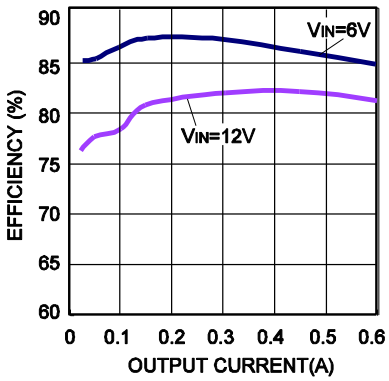
Frequency vs. Junction Temperature



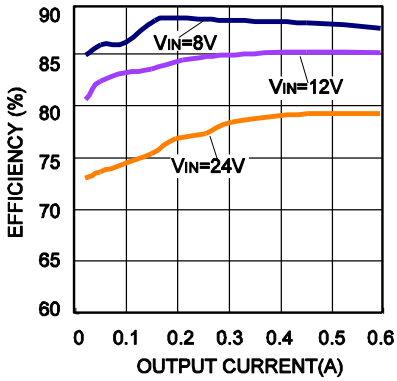
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, C1 = 4.7µF, C2 = 10µF, L = 3.3µH and T_A= 25°C, unless otherwise noted.

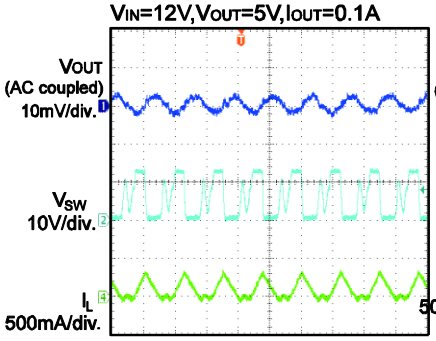
Efficiency
VOUT=2.5V



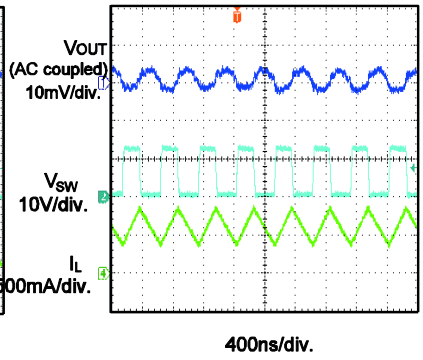
Efficiency
VOUT=3.3V



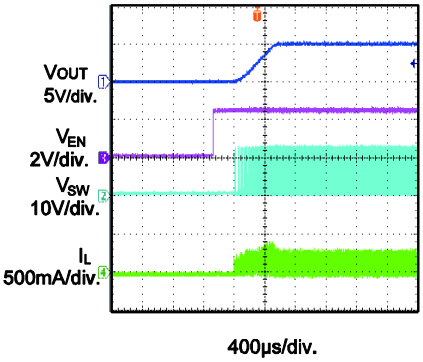
Steady State
VIN=12V,VOUT=5V,IOUT=0.1A



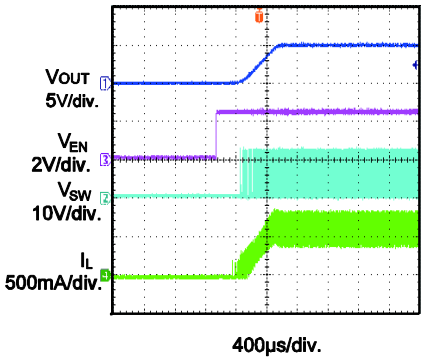
Steady State
VIN=12V,VOUT=5V,IOUT=0.6A



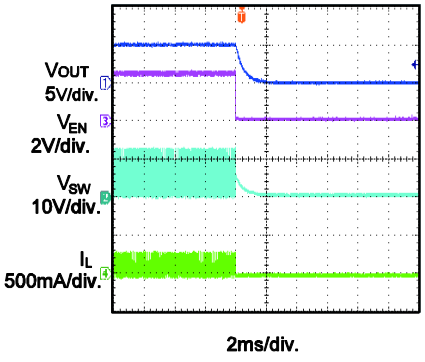
Startup Through EN
VIN=12V,VOUT=5V,IOUT=0.1A



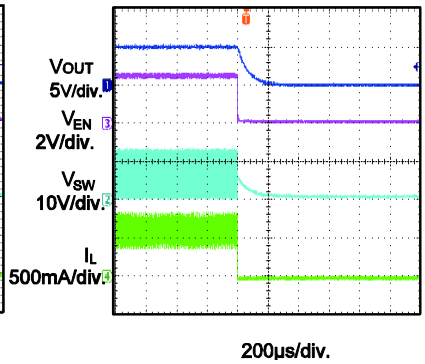
Startup Through EN
VIN=12V,VOUT=5V,IOUT=0.6A



Shutdown Through EN
VIN=12V,VOUT=5V,IOUT=0.1A



Shutdown Through EN
VIN=12V,VOUT=5V,IOUT=0.6A

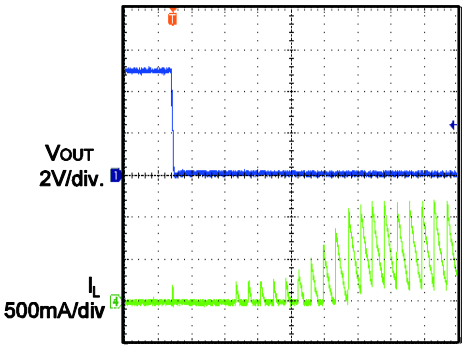


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, C1 = 4.7µF, C2 = 10µF, L = 3.3µH and T_A = 25°C, unless otherwise noted.

Short Circuit Entry

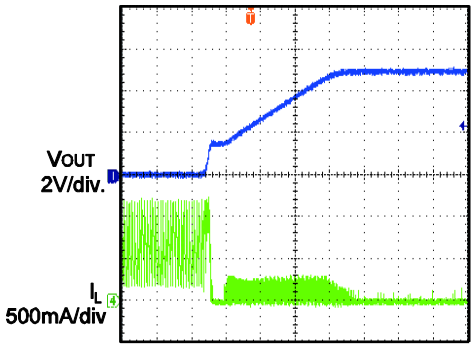
I_{OUT}=0A to Short



20µs/div.

Short Circuit Recovery

I_{OUT}= Short to 0A



100µs/div.

FUNCTIONAL BLOCK DIAGRAM

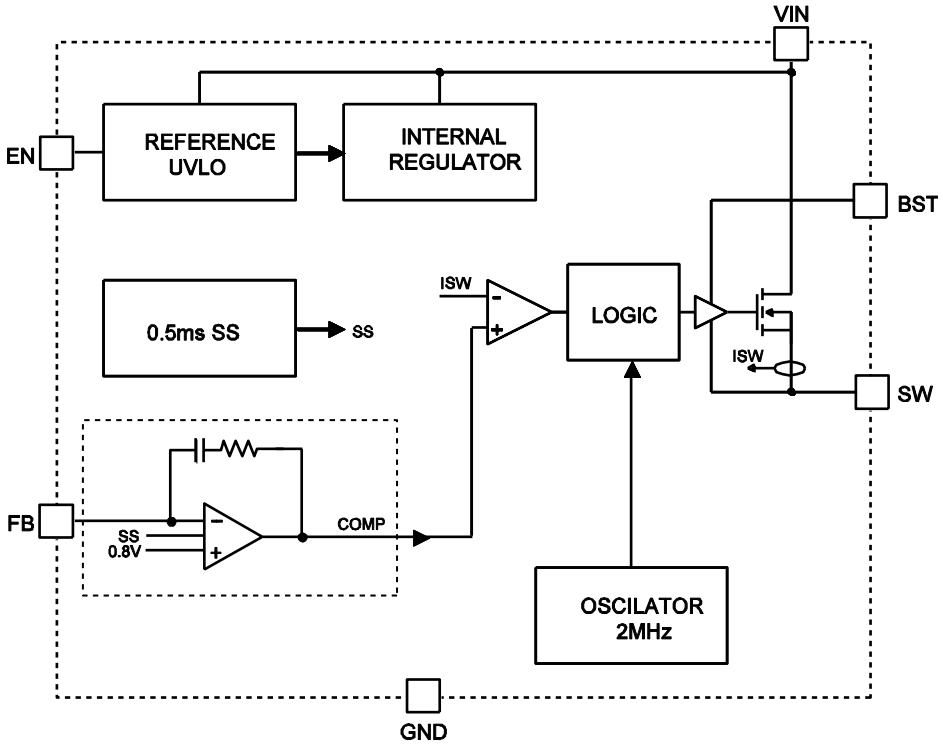


Figure 1: Functional Block Diagram

OPERATION

The MPQ2451 is a 2MHz, non-synchronous, step-down switching regulator with an integrated high-side high voltage power MOSFET. It provides an internally-compensated, highly-efficient output of up to 0.6A with current mode control. It also features wide input voltage range, internal soft-start control, and a precision current limit. Its very low operational quiescent current makes it suitable for battery-powered applications.

PWM Control

At moderate-to-high output current, the MPQ2451 operates in a fixed-frequency peak-current–control mode to regulate the output voltage. A PWM cycle—initiated by the internal clock—turns the power MOSFET on, and the MOSFET remains on until its current reaches the value set by COMP voltage. When the PWM signal goes low, the power switch turns off and remains off for at least 100ns before the next cycle starts.

If the current in the power MOSFET does not reach COMP set current value within one PWM cycle, the power MOSFET remains on to avoid a turn-off operation.

Pulse-Skipping Mode

Under light-load conditions, the MPQ2451 goes into pulse-skipping mode to improve efficiency. Pulse-skipping triggers when the COMP voltage drops below the internal sleep threshold, which generates a PAUSE command to block the turn-on clock pulse so the power MOSFET does not turn ON; this procedure reduces gate driving and switching losses. This PAUSE command causes the whole chip to enter sleep mode, reducing the quiescent current to further improve the light load efficiency.

When the COMP voltage exceeds the sleep threshold, the PAUSE signal resets and the chip resumes normal PWM operation. Whenever the PAUSE changes state from low to high, the PWM signal immediately goes HIGH and turns on the power MOSFET.

Error Amplifier

The error amplifier is composed of an internal op-amp with an RC feedback network connected between its output node (internal COMP node) and its negative input node (FB). When the FB voltage drops below the internal reference voltage (V_{REF}), the op-amp drives the COMP output high, causing a higher switch peak current output and delivering more energy to the output. Conversely, when the FB voltage rises above V_{REF}, the switch peak current output drops.

When using the FB pin, connect to the tap of a voltage divider that is connected between V_{OUT} and GND composed of R_1 and R_2; R_1 also serves to control the gain of the error amplifier in addition to the internal compensation RC network.

Internal Regulator

The 2.6V internal regulator powers most of the internal circuitry. This regulator takes the V_{IN} input and operates in the full VIN range. When V_{IN} is greater than 3.0V, the output of the regulator is in full regulation. When V_{IN} drops below 3.0V, the output degrades.

Enable Control

The MPQ2451 has a dedicated enable control pin, EN. When V_{IN} rises above threshold, the EN pin can enable or disable the chip for HIGH effective logic. Its falling threshold is 1.2V, and its rising threshold is about 1.6V. When floated, the EN pin is internally pulled down to GND to disable the.

When the EN voltage is pulled to 0V, the chip enters the lowest shutdown current mode. When the EN voltage rises above 0V but lower than rising threshold, the chip remains in shutdown mode with a slightly higher shutdown current.

Under Voltage Lockout (UVLO)

V_{IN} under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO rising threshold is approximately 2.9V while its falling threshold is 2.6V.

Internal Soft-start

A reference-type soft-start (SS) prevents the converter-output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (V_{SS}) that ramps up from 0V over the SS time. When V_{SS} is less than V_{REF}, V_{SS} overrides V_{REF} as the error amplifier reference.

The maximum V_{SS} is approximately the same as V_{FB}; i.e. if V_{FB} falls, the maximum of V_{SS} falls. This accommodates short-circuit recovery; when the short-circuit is removed, V_{SS} ramps up to prevent output voltage overshoot.

Thermal Shutdown

Thermal shutdown prevents thermal runaway. When the silicon die temperature exceeds its upper threshold, the entire chip shuts down. When the temperature drops below its lower threshold, the chip is enabled again.

Floating Driver and Bootstrap Charging

The floating power MOSFET driver is powered by an external bootstrap capacitor. This floating driver has its own UVLO protection with a rising threshold of about 2.4V and a falling threshold of about 300mV. During this UVLO, V_{SS} resets to zero. When the UVLO is removed, the controller enters soft-start.

The bootstrap capacitor is charged and regulated to about 5V by the dedicated internal bootstrap regulator. When the voltage between the BST and SW nodes falls below its regulation, a PMOS pass transistor connected from V_{IN} to BST turns on. The charging current path goes from V_{IN}, BST and then to SW. The external circuit must provide enough voltage headroom to facilitate the charging.

If V_{IN} is sufficiently higher than V_{SW}, the bootstrap capacitor will charge. When the power MOSFET is ON, V_{IN} is equal to V_{SW} so the bootstrap capacitor does not charge. Optimal charging occurs when the difference between V_{IN} and V_{SW} reaches its apex when the external freewheeling diode is on. When there is no current in the inductor, SW equals V_{OUT} so the difference between V_{IN} and V_{OUT} can charge the bootstrap capacitor.

At a higher duty cycle, the bootstrap capacitor may not be charged sufficiently because of a shorter charging period. If there is insufficient voltage and time to charge the bootstrap capacitor, add an extra external circuit to ensure the bootstrap voltage in normal operation region.

The floating driver's UVLO is not communicated to the controller.

Make sure the bleed-through current at SW node is at least higher than the floating driver's DC quiescent current of about 20μA.

Current Comparator and Current Limit

A current-sense MOSFET senses the power MOSFET current. This value is input to the high-speed current comparator for current-mode control. When the power MOSFET turns on, the comparator is first blanked to limit noise, and then compares the power switch current against the COMP voltage. When the sensed value exceeds the COMP voltage, the comparator output goes low to turn off the power MOSFET. The maximum current of the internal power MOSFET is internally limited cycle-by-cycle.

Startup and Shutdown

If both V_{IN} and V_{EN} exceed their respective thresholds, the chip starts. The reference block first starts to generate a stable reference voltage and current, and then the internal regulator starts to provide a stable supply for the rest circuit.

While the internal supply rail is up, an internal timer turns the power MOSFET off for about 50μs to blank startup noise. When the internal soft-start block is enabled, it first holds its SS output low to ensure the rest of the circuit is ready before ramping up.

Three events shut down the chip: EN low, V_{IN} low, thermal shutdown. In shutdown procedure, the signaling path is blocked first to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled low. The floating driver is not subject to this shutdown command but its charging path is disabled.

APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The output voltage is set using a resistive voltage divider from the output voltage to the FB pin. The voltage divider sets V_{OUT} and V_{FB} using the following equation:

$$V_{FB} = V_{OUT} \frac{R2}{R1 + R2}$$

Thus the output voltage is:

$$V_{OUT} = V_{FB} \frac{(R1 + R2)}{R2}$$

The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor.

Choose R1 around 124kΩ for optimal transient response. R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.8V} - 1}$$

Table 1: Resistor Selection vs. Output Voltage Setting

V_{OUT}	R1	R2
0.8V	124kΩ (1%)	NS
1.2V	124kΩ (1%)	249kΩ (1%)
3.3V	124kΩ (1%)	40.2kΩ (1%)
5V	124kΩ (1%)	23.7kΩ (1%)

Inductor

The inductor supplies constant current to the output load while being driven by the switched input voltage. A larger-value inductor will result in less ripple current and lower output ripple voltage. However, the larger-value inductor is typically physically larger, has a higher series resistance, or has a lower saturation current.

To determine the inductance, allow the peak-to-peak ripple current in the inductor to be approximately 30% of the maximum load current. Also, chose a peak inductor current below the maximum switch current limit. The inductance value can be calculated by:

$$L1 = \frac{V_{OUT}}{f_S \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, f_S is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated by:

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 \times f_S \times L1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where I_{LOAD} is the load current.

Table 2 lists a number of suitable inductors from various manufacturers. The choice of which style inductor to use mainly depends on the price vs. size requirements and any EMI requirement.

Table 2: Inductor Selection Guide

Part Number	Inductance (µH)	Max DCR (Ω)	Current Rating (A)	Dimensions L x W x H (mm^3)
Wurth Electronics				
7440430022	2.2	0.028	2.5	4.8x4.8x2.8
744043003	3.3	0.035	2.15	4.8x4.8x2.8
7447785004	4.7	0.078	2.4	5.9x6.2x3.2
TOKO				
D63CB-#A916CY-2R0M	2.0	0.019	2.36	6.2x6.3x3.0
D62CB-#A916CY-3R3M	3.3	0.026	2.17	6.2x6.3x3.0
D62CB-#A916CY-4R7M	4.7	0.032	2.1	6.2x6.3x3.0
TDK				
LTF5022T-2R2N3R2	2.2	0.04	3.2	5.2x5.0x2.2
LTF5022T-3R3N2R5	3.3	0.06	2.5	5.2x5.0x2.2
LTF5022T-4R7N2R0	4.7	0.081	2.0	5.2x5.0x2.2
COOPER BUSSMANN				
SD25-2R2	2.2	0.031	2.8	5.2x5.2x2.5
SD25-3R3	3.3	0.038	2.21	5.2x5.2x2.5
SD25-4R7	4.7	0.047	1.83	5.2x5.2x2.5

The input capacitor (C1) can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, add a small, high quality ceramic capacitor—for example, a 0.1µF—as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Output Capacitor

The output capacitor (C2) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right)$$

Where L is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system.

Compensation Components

The goal of compensation design is to shape the converter transfer function to get a desired loop gain. Lower crossover frequencies result in slower line and load transient responses, while higher crossover frequencies can cause system instability. Generally, set the crossover frequency to equal approximately one-tenth of the switching frequency. If using an electrolytic capacitor, select a loop bandwidth is no higher than 1/4 of the ESR zero frequency (f_{ESR}), where f_{ESR} is given by:

$$f_{ESR} = \frac{1}{2\pi \times C2 \times R_{ESR}}$$

The Table 3 lists the typical values of compensation components of some standard output voltages with various output capacitors (ceramic) and inductors. The values of the compensation components have been optimized for fast transient responses and good stability under the given conditions.

Table 3: Compensation Values for Typical

V_{OUT} (V)	L (μH)	C2 (μF)	R2 (kΩ)	C3 (pF)
1.2	2.2	10	249	22
2.5	2.2	10	57.6	22
3.3	2.2	10	40.2	33
5	3.3	10	23.7	33
12	6.2	10	8.87	47

Note:
With the compensation, the control loop has the bandwidth at about 1/10 switching frequency and the phase margin higher than 45 degree.

External Bootstrap Diode

An external bootstrap diode may enhance the efficiency of the regulator. Connect an external BST diode from 5V to the BST pin if:

- There is a 5V rail available to the system;
- $V_{IN} \leq 5V$;
- $3.3V < V_{OUT} < 5V$;

This diode is also recommended for high-duty–cycle ($V_{OUT}/V_{IN} > 65\%$) applications.

A low-cost bootstrap diode, such as IN4148 or BAT54, is suitable for such applications.

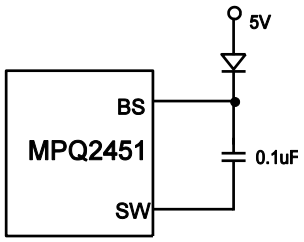


Figure 2: External Bootstrap Diode

At no load or light load, the converter may operate in pulse-skipping mode in order to regulate the output voltage and leave less time to refresh the BST voltage. To ensure sufficient gate voltage, select (V_{IN} - V_{OUT}) > 3V. For example, if V_{OUT} is 3.3V, V_{IN} needs to be higher than 3.3V+3V=6.3V at no load or light load. To meet this requirement, the EN pin can be used to program the input UVLO voltage to V_{OUT}+3V.

PCB Layout

PCB layout requires high-frequency noise considerations to limit voltage spikes on the SW node and to limit EMI noise. Keep the path of the input decoupling capacitor, catch diode, the V_{IN} pin, SW pin, and PGND as short as possible using short and wide traces, with the passive components as close to the device as possible.

Run the feedback trace far from the inductor and noisy power traces: if possible, run the feedback trace on the opposite side of the PCB from the inductor, separated by a ground plane. Expect greater switching losses at high switching frequencies.

Add a grid of thermal vias under the exposed pad to improve thermal conductivity. Use small vias (15mil barrel diameter) so that the hole fills during the plating process, and to avoid solder wicking during the reflow process associated with larger vias. Use a pitch (distance between the centers) of approximately 40mil between the thermal vias. Please refer to the layout example on EVQ2451 datasheet.

TYPICAL APPLICATION CIRCUITS (SOT23-6L)

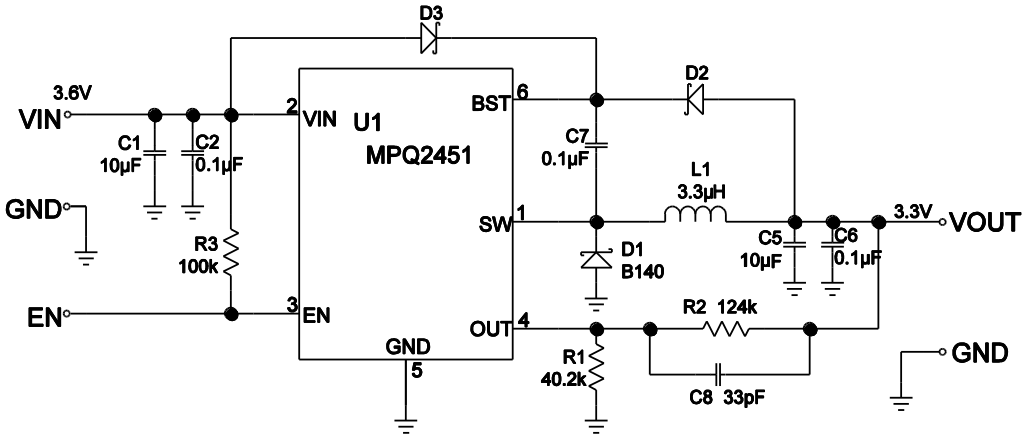


Figure 3: Low Input Voltage With Boost Diode Application Schematic

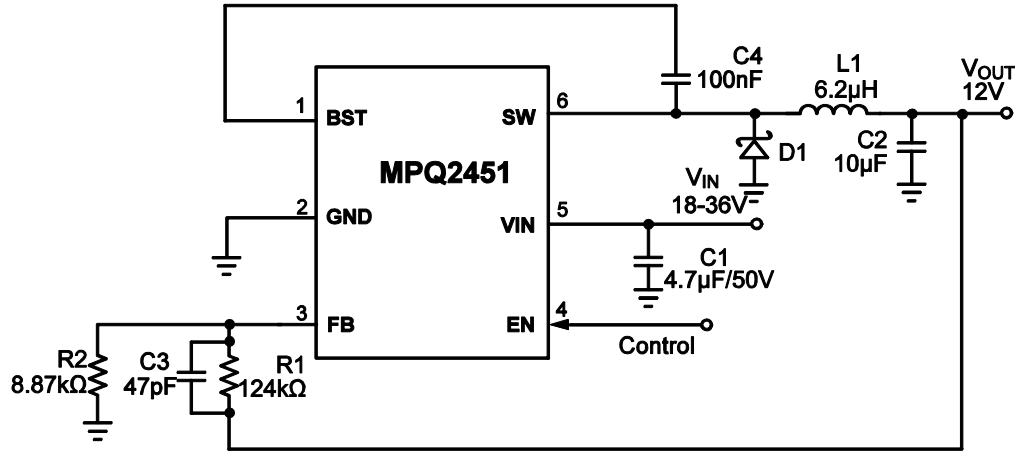
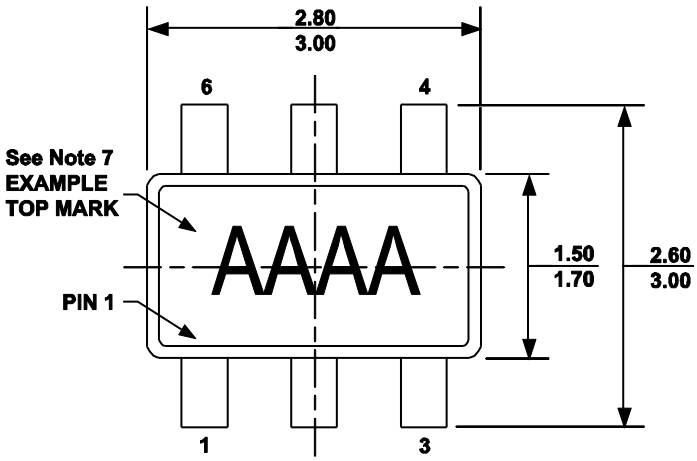


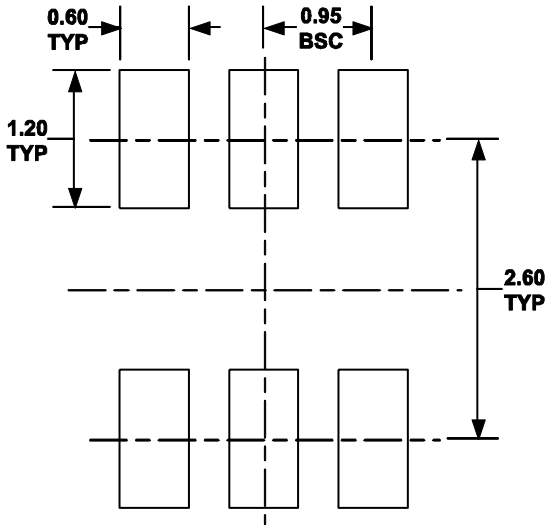
Figure 4: 12V Output Typical Application Schematic

PACKAGE INFORMATION

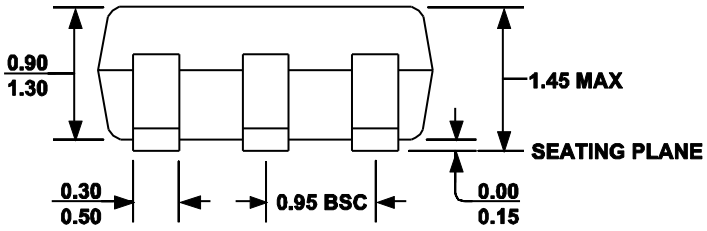
SOT23-6L



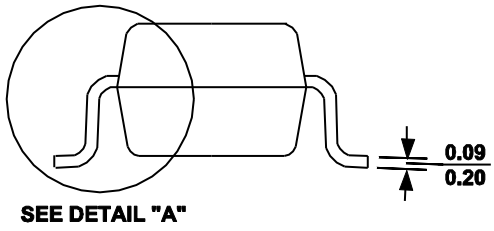
TOP VIEW



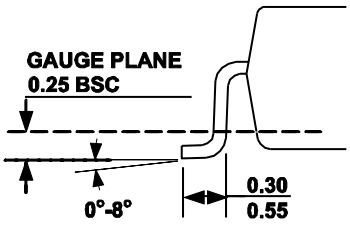
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

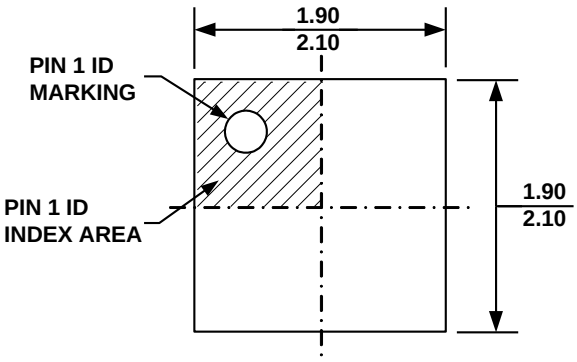


DETAIL "A"

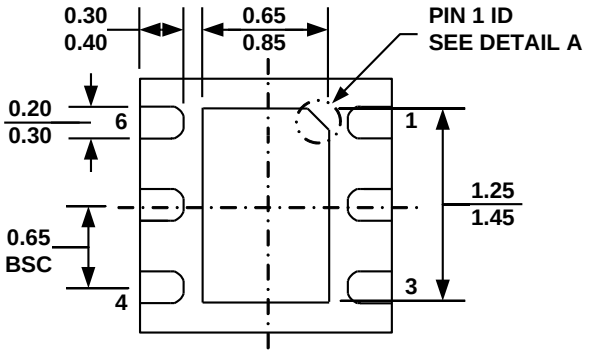
NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-178, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

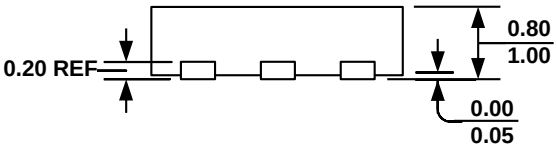
QFN6 (2mmx2mm)



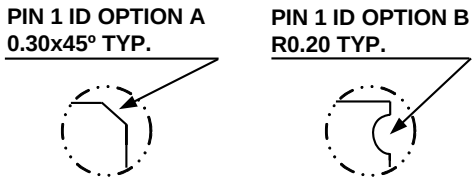
TOP VIEW



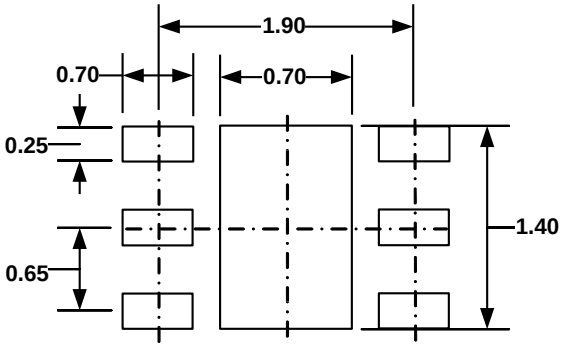
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN