56F800 Demonstration Board

User Manual

56F800
16-bit Digital Signal Controllers

DSP56F800DBUM
Rev. 0
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Preface

This reference manual describes in detail the hardware on the 56F800 Demonstration Board.

Audience

This document is intended for application developers who are creating software for devices using the Freescale 56F800 Demonstration Board.

Organization

This manual is organized into two chapters and one appendix.

- **Chapter 1, Introduction -** provides an overview of the Demonstration Board and its features.
- Chapter 2, Technical Summary - describes the 56F800 Demonstration Board in detail.
- **Appendix A, 56F800 Demonstration Board Schematics -** contains the schematics of the 56F800 Demonstration Board.

Suggested Reading

Related documentation for the 56F800 family of digital signal controllers may be found at:

http://www.freescale.com/dsc

Notation Conventions

This manual uses the following notational conventions:

Typeface, Symbol or Term	Meaning	Examples	Typeface, Symbol or Term
`Courier Monospaced Type`	Code examples	`//Process command for line flash`	`Courier Monospaced Type`
Italic	Directory names, project names, calls, functions, statements, procedures, routines, arguments, file names, applications, variables, directives, code snippets APIs in text	...and contains these core directories: *applications* contains applications software... ...CodeWarrior project, *3des.mcp* is... ...the *pConfig* argument.... ...defined in the C header file, *aec.h*....	*Italic*
Bold	Reference sources, paths, emphasis	...refer to the **Targeting DSP56F80x Platform** manual.... ...see: **C:\Program Files\Embedded SDK\help\tutorials**	**Bold**
Blue Text	Linkable	...refer to Chapter 7, License....	Blue Text
Number	Any number is considered a positive value, unless preceded by a minus symbol to signify a negative value	3V -10 DES^{-1}	Number
ALL CAPITAL LETTERS	# defines/ defined constants	# define INCLUDE_STACK_CHECK	ALL CAPITAL LETTERS
Brackets [...]	Function keys	...by pressing function key [F7]	Brackets [...]

Cautionary Notes

1. Electrostatic Discharge (ESD) prevention measures should be applied whenever handling this product. ESD damage is not a warranty repair item.
2. EMC Information on the 56F800 Demonstration Board:
    a. This product as shipped from the factory with associated power supplies and cables, has been tested and meets with requirements of CE and the FCC as a CLASS A product.
    b. This product is designed and intended for use as a development platform for hardware or software in an educational or professional laboratory.
    c. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate prevention measures.
    d. Attaching additional wiring to this product or modifying the products operation from the factory default as shipped may effect its performance and also cause interference with other apparatus in the immediate vicinity. If such interference is detected, suitable mitigating measures should be taken.

Terminology

This development board applies option selection jumpers. Terminology for application of the option jumpers is as follows:

Jumper on, in, or installed = jumper is a plastic shunt that fits across 2 pins and the shunt is installed so that the 2 pins are connected with the shunt.

Jumper off, out, or idle = jumper or shunt is installed so that only 1 pin holds the shunt, no 2 pins are connected, or jumper is removed. It is recommended that the jumpers be idled by installing on 1 pin so they will not be lost.

This development board applies CUT_AWAY option selections. These option selections apply surface mount resistor locations with a printed circuit board trace connecting both component pads. This type connection places an equivalent 0-ohm type resistor in series with the I/O signal and the user component or I/O connector on the board. These connections maybe cut with a razor blade or similar type knife between the component pads to isolate the default connection provided. Reconnection of the cut-away type pads can be made by either installing a 0 ohm 0805 size surface mount resistor or a small wire jumper on the component pads.

Definitions, Acronyms, and Abbreviations

Definitions, acronyms and abbreviations for terms used in this document are defined below for reference.

ADC	Analog-to-Digital Converter
CTS	Clear To Send
ESD	Electrostatic Discharge
GPIO	General Purpose Input and Output Port
JTAG	Joint Test Action Group. A bus protocol/interface used for test and debug.
OnCE™	On-Chip Emulation, a debug bus and port created by Freescale to enable designers to create a low-cost hardware interface for a professional quality debug environment.
PC	Personal Computer
POT	Potentiometer
PWM	Pulse Width Modulation
RTS	Request To Send

References

The following sources were referenced to produce this manual:

DSP56800 Family Manual

DSP56F80x User's Manual

Technical Data, 56F801 16-Bit Digital Signal Controller

Chapter 1
Introduction

The 56F800 Demonstration Board is used to demonstrate the abilities of the 56F800 family and to provide a hardware tool allowing the development of applications that use the 56F800 devices.

1.1 56F800 Demonstration Board Features

- 56F801FA60 (60 MHz version)
- RESET Switch
- IRQ Switch
- GPIO / SERIAL Port (10 pin) *
- TIMER / PWM Port (10 Pin) *
- ADC Port (10 Pin) *
- JTAG / OnCE Port (14 pin) *
- Host JTAG Port (P1- DB25P)
- COM1 Port - SCI to RS232 (DB9S) *
- PWR Jack supply connector
- Power Port *
- Power Indicator
- 10 User Indicators
- User Potentiometer (R12)
- Microphone with amplifier
- Crystal Reference (Y1) *

* All components may not be installed at the factory. The user may install the components to apply associated feature.

The 56F800 Demonstration Board is detailed in **Figure 1-1**.

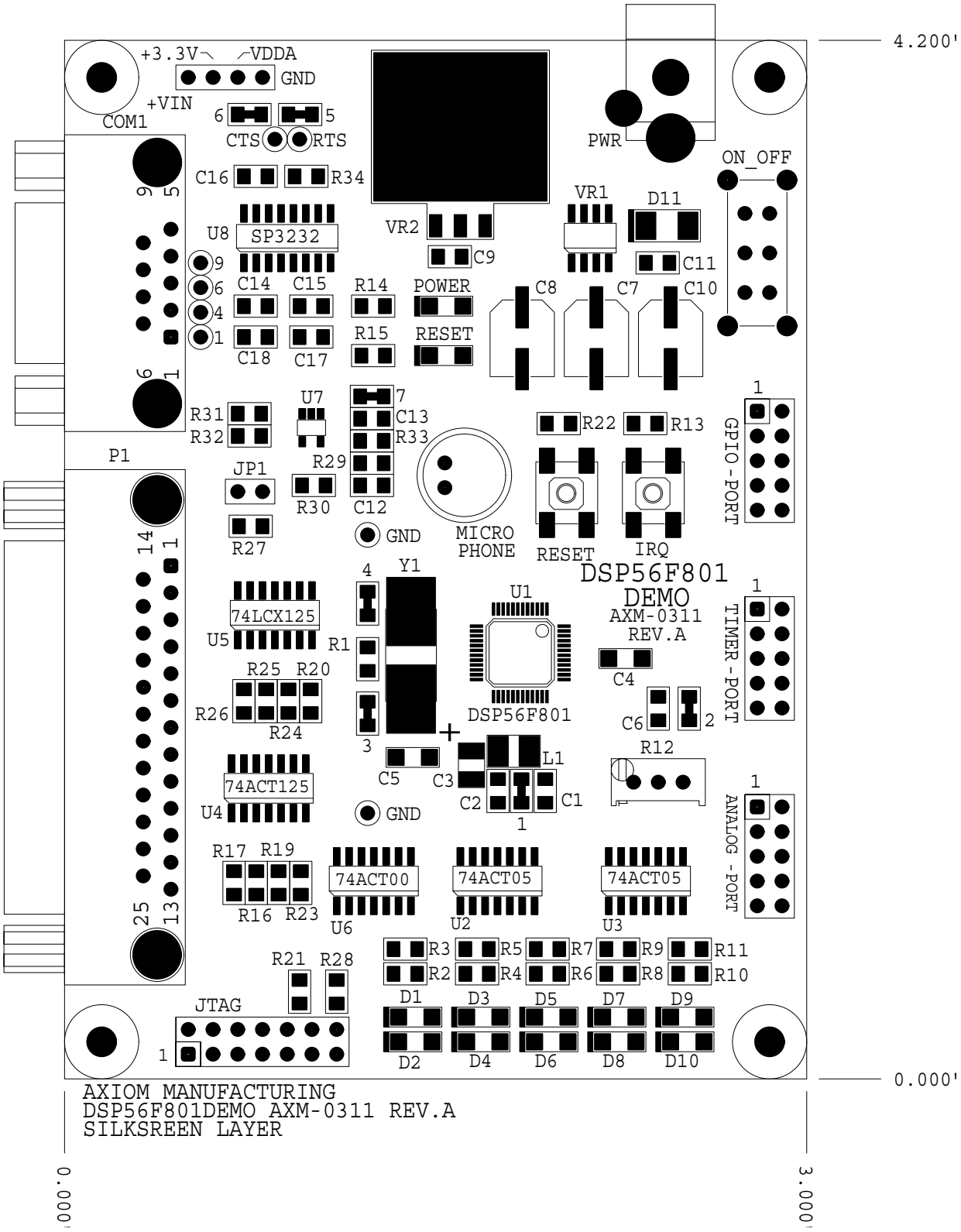

Figure 1-1. 56F800 Demonstration Board

1.2 SPECIFICATIONS

- +9V DC input voltage typical, 200ma
- Input voltage range: +7 to +15V DC
- On board regulated +5V DC and +3.3V DC supplies
- Board size: 3 x 4.2 inches

Chapter 2
Technical Summary

This chapter describes the 56F800 Demonstration Board's available options.

2.1 OPTIONS

2.1.1 HOST_ENABLE

The HOST_ENABLE option jumper is installed by default and enables the Host JTAG interface on the board. With the option jumper installed, the 56F801 device will reset into Debug mode and await Host commands on the Host JTAG port (P1). Removing the HOST_ENABLE option jumper will allow the 56F801 device to reset normally and execute program code contained in the device's Flash memory.

- **HOST_ENABLE = INSTALLED:** Debug Mode; host JTAG port is active
- **HOST_ENABLE = OPEN or IDLE:** Normal Mode; executes user code in Flash

2.1.2 CUT_AWAY Options

CUT_AWAY options allow the user to disconnect dedicated 56F801 I/O port resources from development board connectors or peripherals. The CUT_AWAY options also allow for re-establishing the connection by installing surface-mount 0805-size 0 ohm resistors or mod wire with the use of a soldering iron. Normal operation of the 56F800 Demonstration Board generally does not require any manipulation of the CUT_AWAY options.

Table 2-1. CUT_AWAY Options

CUT_AWAY #	Description	56F801 Signal	Connection Signal
1	ADC reference supply	V_{REF}	V_{DDA}
2	User POT (R12) to ADC	ANA6	R12 wiper
3	Crystal oscillator isolation	XTAL / GPIOB3	GPIO / SERIAL pin 4

Table 2-1. CUT_AWAY Options (Continued)

CUT_AWAY #	Description	56F801 Signal	Connection Signal
4	Crystal oscillator isolation	EXTAL / GPIOB2	GPIO / SERIAL pin 3
5	COM1 serial port	TXD0 / GPIO0	U8 pin 11 (COM1 TXD)
6	COM1 serial port	RXDO / GPIOB1	U8 pin 12 (COM1 RXD)
7	Microphone to ADC	ANA2	U7 pin 4 (Microphone output)

2.2 PORTS AND CONNECTORS

2.2.1 PWR Jack

This connector provides power input to the board by default. The PWR jack accepts a standard 2.0 ~ 2.1mm center-barrel plug connector (positive voltage center) to provide the +VIN supply of +9V DC at 200ma.

2.2.2 POWER PORT

Provides access to the +9V DC input, GND (power ground), +5V DC and +3.3V DC power supplies. The +9V DC input should only be applied by PWR jack or Power Port, but not both, or a supply conflict may occur and the 56F800 Demonstration Board could be damaged. Power Port accepts a 3.5mm pin space terminal block.

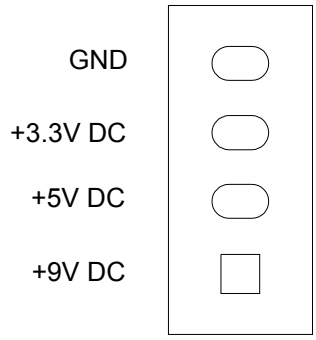

Figure 2-1. Power Port

2.2.3 GPIO / SERIAL

TXD0 / GPIOB0	1	2	GPIOB1 / RXD0
GPIOB2	3	4	GPIOB3
SCLK / GPIOB4	5	6	GPIOB5 / MOSI
MISO / GPIOB6	7	7	GPIOB7 / SS*
IREQA*	9	10	RESET*

GPIO B port provides alternate functions as SCI (COM1 and indications) and SPI ports. IREQ and RESET signals are also provided on this connector.

2.2.4 TIMER / PWM

TD0 / GPIOA0	1	2	GPIOA1 / TD1
TD2 / GPIOA2	3	4	FAULTA0
PWMA4	5	6	PWMA5
PWMA2	7	7	PWMA3
PWMA0	9	10	PWMA1

GPIOA0 - 2 port provides alternate functions of Timer TD0 - 2 I/O.
Note that most of these ports provide a user indication.

2.2.5 ADC Port

ANA6	1	2	ANA7
ANA4	3	4	ANA5
ANA2	5	6	ANA3
ANA0	7	7	ANA1
VREF	9	10	GND

Analog inputs. Note that ANA2 and ANA6 provide Microphone and User POT R12 input, respectively.

2.2.6 COM1

1	1		
TXD0	2	6	6
RXD0	3	7	CTS
4	4	8	RTS
GND	5	9	9

The **COM1** port has a female DB9 connector that interfaces to the 56F801 internal SCI0 serial port via the U8 RS-232 transceiver. It uses a simple 2-wire asynchronous serial interface and is translated to RS-232 signaling levels.
1,4,6 connected (host null)

RTS and CTS flow control connection pads are provided on the 56F800 Demonstration Board to apply unassigned 56F801 I/O to support flow control on COM1. The RTS pad provides RS-232 level output conversion to COM1 port pin 8. The CTS pad provides RS-232-converted input from COM1 pin 7.

The 1, 4, 6, and 9 pins provide RS-232 status. The 1, 4, and 6 pins are connected on the bottom of the development board to provide NULL status to the host. The user may isolate pins and provide the status connections to the host by applying I/O signals and RS-232 level conversion.

2.2.7 JTAG / OnCE

The JTAG 14-pin connector is compatible with the Freescale OnCE development port. This connector allows the connection of a OnCE-style background debug cable for software development, programming and debugging in real time.

TDI	1	2	GND
TDO	3	4	GND
TCK	5	6	GND
	7	7	(key)
RESET in	9	10	TMS
+3.3V DC	11	12	
DE*	13	14	TRST* in

JTAG / OnCE BDM connection.

Note: HOST_ENABLE option must be open or idle to apply this connector.

2.2.8 P1 - HOST JTAG

The P1 - Host JTAG connector provides development port interface to a hosting Personal Computer's LPT or Printer port. The HOST_ENABLE option jumper must be installed for this port to operate.

	1	14	
Reset in	2	15	Pin 8 tie
TMS	3	16	GND
TCK	4	17	
TDI	5	18	GND
TRST*	6	19	GND
DE* (Note R23)	7	20	GND
Pin 15 tie	8	21	GND
	9	22	GND
	10	23	GND
TDO	11	24	GND
	12	25	GND
P-CON	13		

P1 - HOST JTAG connector is a DB25 pin connector. Signals are organized for direct connection to an IBM-compatible PC with a straight-through DB25 cable.

Pin 7 / DE* signal, if supported, can be enabled by installing R23 (51 ohms)

Note: HOST_ENABLE option must be installed to apply this connector.

2.3 USER FEATURES

Several circuits are provided for demonstration of 56F800 applications.

2.3.1 MICROPHONE

A microphone with audio amplifier is provided on the 56F800 Demonstration Board for user applications. The amplifier provides low-pass filtering starting at ~4000Hz for speech input. The audio signal from the microphone amplifier is provided to the ADC ANA2 input channel via CUT_AWAY option #7.

2.3.2 POTENTIOMETER (POT) - R12

The user POT R12 provides a 0 to +3.3V adjustable analog input to the 56F801's ADC ANA6 channel. R12 can be removed from the ANA6 channel by CUT_AWAY option #2.

2.4 Indicators

User indicactions are provided that are active with a high level on the associated 56F801 device's I/O port. **Table 2-2** details the indicators.

Table 2-2. Indicators

Indicator	56F800 Signal	Color
D1	PWMA0	Green
D2	PWMA1	Green
D3	PWMA2	Green
D4	PWMA3	Green
D5	PWMA4	Yellow
D6	PWMA5	Yellow
D7	GPIOB1 / RXD0	Yellow
D8	GPIOB0 / TXD0	Yellow
D9	GPIOA1 / TD1	Red
D10	GPIOA2 / TD2	Red

Appendix A
56F800 Demonstration Board Schematics

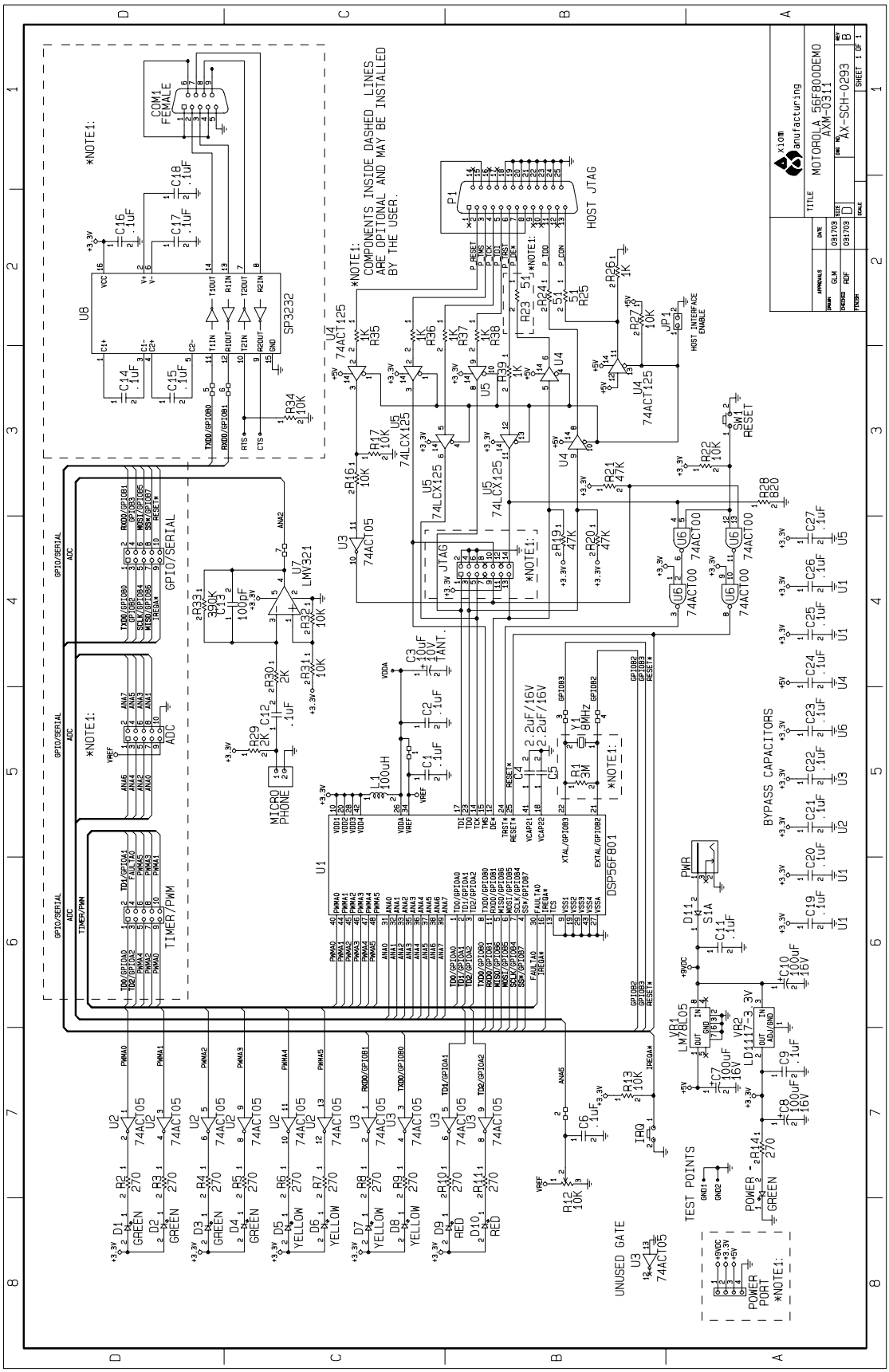

Figure A-1. 56F800 Demonstration Board

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