MMB Networks EM357 ZigBee Module

RapidConnect

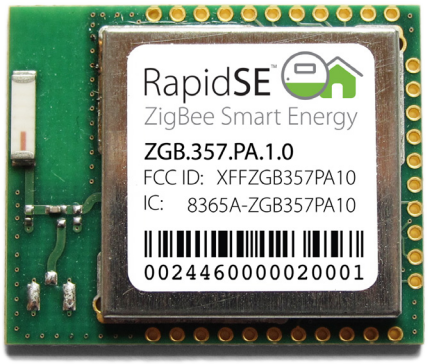
Z357PA10-SMT, Z357PA10-USN, Z357PA10-UFL

Document Rev 4.0

The MMB Networks EM357 ZigBee Module is a drop-in ZigBee Smart Energy and Home Automation solution. Preloaded with MMB Networks' RapidSE ZigBee Smart Energy application or RapidHA Home Automation application, it offers hardware vendors an easy way to integrate a fully-implemented, automated ZigBee Smart Energy or ZigBee Home Automation platform into their existing devices.

MMB Networks offers a variety of hardware and software development tools to facilitate integration. For more information, please visit

http://www.mmbnetworks.com



Contents

1 | General Information

Note that some of the specifications refer to either EM357 or Module. Please note specifications cited as EM357 are taken from the EM357 datasheet (this should also be noted where referred to). Module means measurements taken with our production module.

2 | Memory

SKU	RAM (kB)	On-Chip Flash (kB)	Serial Flash (kB)
ZGB.357.PA.1.0	12	192	512

3 | Module Pinout

Module Pad	Function	EM357 GPIO (EM357 Pin Number)
1	GND	
2	Module UART RX	PB2 (31)
3	Module UART TX	PB1 (30)
4		PB4 (20)
5		PB3 (19)
6		PA5 (27)
7		PA4 (26)
8		PC1 (38)
9		PB0 (36)
10	VCC	
11	GND	
12	Host Controlled Handshake Line	PB4 (20)
13	Module Controlled Handshake Line	PA6 (29)
14	SPI Slave CLK	PB3 (19)
15	SPI Slave In	PB2 (31)
16	SPI Slave Out	PB1 (30)
17	Reset Module, active low	nReset (12)
18	VCC	
19	GND	
20	n.c.	
21	n.c.	
22	GND	
23	Reset Module, active low	nReset (12)
24		JTCK (32)
25		JTDO, PC2 (33)
26		JTDI, PC3 (34)
27		JTMS, PC4 (35)
28		JRST, PC0 (40)

Module Pad	Function	EM357 GPIO (EM357 Pin Number)
29		PB7 (41)
30	n.c.	
31	n.c.	
32	GND	

3.1 | Debug and Programming Interface

In order to access the EM357 for programming and debug purposes, it is recommended that the designer incorporate Ember's 10-pin InSight Port connector. This will allow Ember's InSight Adapter (ISA3) to be used. Contact Ember for details regarding the InSight Port connector and ISA3.

The following table shows a pin mapping between Ember's 10-pin InSight Port connector and the module, and the graphic to the right displays the layout of the InSight Port connector.

Ember InSight Port Pin	Module Pin
1	10, 18 (VCC)
2	25 (PC2 / JTDO / SWO)
3	28 (PC0 / JRST)
4	26 (PC3 / JTDI)
5	1, 11, 19, 22, 32 (GND)
6	24 (JTCK)
7	27 (PC4 / JTMS / SWDIO)
8	17, 23 (nReset)
9	7 (PA4 / PTF)
10	6 (PA5 / PTD)

VBRD	1	2	PC2 (JTDO/SWO)
PC0 (nJRST)	3	4	PC3 (JTDI)
GND	5	6	JCLK/SWCLK
PC4 (JTMS/SWDIO)	7	8	nRESET
PA4 (PTF)	9	10	PA5 (PTD)

4 | **Electrical Specifications**

4.1 | Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units
Supply Voltage (VCC)	0	3.6	V
Voltage on any GPIO ([PA[0:7], PB[0:7], PC[0:7]), JTCK, nReset	-0.3	VCC + 0.3	V
Voltage on any GPIO pin (PA4, PA5, PB5, PB6, PB7, PC1) when used as an input to the general purpose ADC with the low voltage range selected	-0.3	2	V
Ambient Operating Temperature	-40	85	°C

4.2 | Recommended Operating Conditions

Parameter	Minimum	Typical	Maximum	Units
Supply Voltage (VCC)	2.7	3.3	3.6	V
Temperature Range	-40		85	°C

4.3 | DC Electrical Characteristics

Parameter	Test Condition	Minimum	Typical	Maximum	Units
TX current	At 25 °C, VCC = 3.3v, boost mode		208		mA
TX current	At 25 °C, VCC = 3.3v, normal mode		205		mA
RX current	At 25 °C, VCC = 3.3v		28		mA
Idle current	At 25 °C, VCC = 3.3v, sleep mode		8.5		mA
Deep sleep current	At 25 °C, VCC = 3.3v, shutdown mode		0.65		µA
Low Schmitt switching threshold	Schmitt input threshold going from high to low	0.42 x VCC		0.5 x VCC	V
High Schmitt switching threshold	Schmitt input threshold going from low to high	0.62 x VCC		0.8 x VCC	V
Input current for logic 0				-0.5	µA
Input current for logic 1				0.5	µA
Input pull-up resistor value		24	29	34	kΩ
Input pull-down resistor value		24	29	34	kΩ
Output voltage for logic 0		0		0.18 x VCC	V
Output voltage for logic 1		0.82 x VCC		VCC	V
Output source current (standard current pad)				4	mA
Output sink current (standard current pad)				4	mA
Output source current, high current pad: PA6, PA7, PB6, PB7, PC0				8	mA
Output sink current, high current pad: PA6, PA7, PB6, PB7, PC0				8	mA
Total output current (for I/O Pads)				40	mA

5 | **RF Specifications**

5.1 | Receive Specifications

Module Receive Characteristics

Parameter	Test Condition	Min	Typical	Max	Units
Receive sensitivity	Max gain		TBD		dBm
Receive sensitivity (Boost)	Max gain		TBD		dBm
Input 1dB Compression	CW		26		dBm
Input IP3	Two –7 dBm CW tones spaced 1 MHz apart		36		dBm

EM357 Receive Characteristics

This table lists the key parameters of the integrated IEEE 802.15.4-2003 receiver on the EM357. This information is taken from the Ember EM357 Datasheet. This document is available at:
http://www.silabs.com/Support%20Documents/TechnicalDocs/EM35x.pdf

Note: Receive measurements were collected with Ember's EM35x Ceramic Balun Reference Design (Version A0) at 2440MHz. The Typical number indicates one standard deviation above the mean, measured at room temperature (25°C). The Min and Max numbers were measured over process corners at room temperature.

Parameter	Test Condition	Min	Typical	Max	Units
Frequency range		2400		2500	MHz
Sensitivity (boost mode)	1% PER, 20 byte packet defined by IEEE 802.15.4-2003		-102	-96	dBm
Sensitivity	1% PER, 20 byte packet defined by IEEE 802.15.4-2003		-100	-94	dBm
High-side adjacent channel rejection	IEEE 802.15.4-2003 signal at – 82 dBm		35		dB
Low-side adjacent channel rejection	IEEE 802.15.4-2003 signal at – 82 dBm		35		dB
2nd high-side adjacent channel rejection	IEEE 802.15.4-2003 signal at – 82 dBm		46		dB
2nd low-side adjacent channel rejection	IEEE 802.15.4-2003 signal at – 82 dBm		46		dB
High-side adjacent channel rejection	Filtered IEEE 802.15.4-2003 signal at – 82 dBm		39		dB
Low-side adjacent channel rejection	Filtered IEEE 802.15.4-2003 signal at – 82 dBm		47		dB
2nd high-side adjacent channel rejection	Filtered IEEE 802.15.4-2003 signal at – 82 dBm		49		dB
2nd low-side adjacent channel rejection	Filtered IEEE 802.15.4-2003 signal at – 82 dBm		49		dB
High-side adjacent channel rejection	CW signal at – 82 dBm		44		dB
Low-side adjacent channel rejection	CW signal at – 82 dBm		47		dB
2nd high-side adjacent channel rejection	CW signal at – 82 dBm		59		dB
2nd low-side adjacent channel rejection	CW signal at – 82 dBm		59		dB
Channel rejection for all other channels	IEEE 802.15.4-2003 signal at – 82 dBm		40		dB
802.11g rejection centered at + 12MHz or - 13MHz	IEEE 802.15.4-2003 signal at – 82 dBm		36		dB
Maximum input signal level for correct operation		0			dBm
Co-channel rejection	IEEE 802.15.4-2003 signal at – 82 dBm		-6		dBc
Relative frequency error (2x40 ppm required by IEEE 802.15.4-2003)		-120		120	ppm

Parameter	Test Condition	Min	Typical	Max	Units
Relative timing error (2x40 ppm required by IEEE 802.15.4-2003)		-120		120	ppm
Linear RSSI range	As defined by IEEE 802.15.4-2003	40			dB
RSSI Range		-90		-40	dB

5.2 | Transmit Specifications

Parameter	Test Condition	Min	Typical	Max	Units
Output Power at highest power setting (boost mode)			20		dBm
Output Power at highest power setting (to comply with EU regulations)	EM357 set to -7 dBm power level		10		dBm
Output Power at lowest power setting			-55		dBm
Error vector magnitude as per IEEE 802.15.4			5	15	%
Carrier frequency error		-40		40	ppm
PSD Mask relative	3.5 MHz distance from carrier	-20			dB
PSD Mask absolute	3.5 MHz distance from carrier	-30			dBm

5.3 | Synthesizer

EM357 Synthesizer Parameters

This table lists the key parameters of the integrated synthesizer on the EM357. Taken from the EM357 datasheet.

Parameter	Test Condition	Min	Typical	Max	Units
Frequency range		2400		2500	MHz
Frequency resolution			11.7		kHz
Lock time	From off			100	µs
Relock time	Channel change or Rx/Tx turnaround (IEEE 802.15.4-2003 defines 192µs turnaround time)			100	µs
Phase noise at 100kHz offset			-75		dBc/Hz
Phase noise at 1MHz offset			-100		dBc/Hz
Phase noise at 4MHz offset			-108		dBc/Hz
Phase noise at 10MHz offset			-114		dBc/Hz

6 | **Functional Specifications**

6.1 | Serial Ports

Refer to the EM357 data sheet for functionality and associated GPIO pin outs.

Note: The module pin out table in section 2 of this document provides a cross reference between the MMB PA module pins and the EM357 GPIO.

6.1.1 | SC1 Serial Controller (UART, SPI, TWI)

The SC1 module provides UART, SPI (master or slave), or TWI (master) serial communications.

Serial Controller Features

The SC1 UART supports the following features:

- Baud rate (300 bps up to 921.6 kbps) (**Note: these values are provided to show the hardware capability. RapidSE does not provide the ability to modify the baud rate from the default value of 115.2 kbps. However, MMB can adjust it as necessary through a Non-Recurring Engineering engagement)*
- Data bits (7 or 8)
- Parity bits (none, odd, or even)
- Stop bits (1 or 2)
- False start bit and noise filtering
- Receive and transmit FIFOs
- Optional CTS/RTS flow control
- Receiver and transmit DMA channels
- GPIO signals:
  - TXD (serial data out)
  - RXD (serial data in)
  - nRTS (optional)
  - nCTS (optional)

The SPI slave controller has the following features:

- Full duplex operation
- Up to 4 Mbps data transfer rate
- Programmable clock polarity and clock phase
- Selectable data shift direction (either LSB or MSB first)
- Slave select input
- The following signals can be made available on the GPIO pins:
  - MOSI (serial data in)
  - MISO (serial data out)
  - SCLK (serial clock in)
  - nSSEL (slave select)

The SPI master controller has the following features: *(*Note: the SPI master controller data is provided to show the hardware capability. RapidSE is configured as a SPI Slave, not Master)*

- Full duplex operation
- Programmable clock frequency (12 MHz max.)
- Programmable clock polarity and clock phase
- Selectable data shift direction (either LSB or MSB first)
- Receive and transmit FIFOs
- Receive and transmit DMA channels
- The following signals can be made available on the GPIO pins:
  - MOSI (serial data out)
  - MISO (serial data in)
  - MCLK (serial clock out)

Both EM35x serial controllers SC1 and SC2 include a Two Wire serial Interface (TWI) master controller with the following features: (**Note: Current MMB modules are not configured to support TWI/I2C. Please contact MMB for further information.*)

- Uses only two bidirectional GPIO pins
- Programmable clock frequency (up to 400 kHz)
- Supports 7-bit and 10-bit addressing
- Compatible with Philips I^2C-bus slave devices
- The following signals can be made available on the GPIO pins:
  - SDA (bidirectional serial data)
  - SCL (bidirectional serial clock)

6.2 | GPIO

The EM357 has multi-purpose GPIO pins that may be individually configured as:

- General purpose output
- General purpose open-drain output
- Alternate output controlled by a peripheral device
- Alternate open-drain output controlled by a peripheral device
- Analog
- General purpose input
- General purpose input with pull-up or pull-down resistor

6.3 | Analog to Digital Converter (ADC)

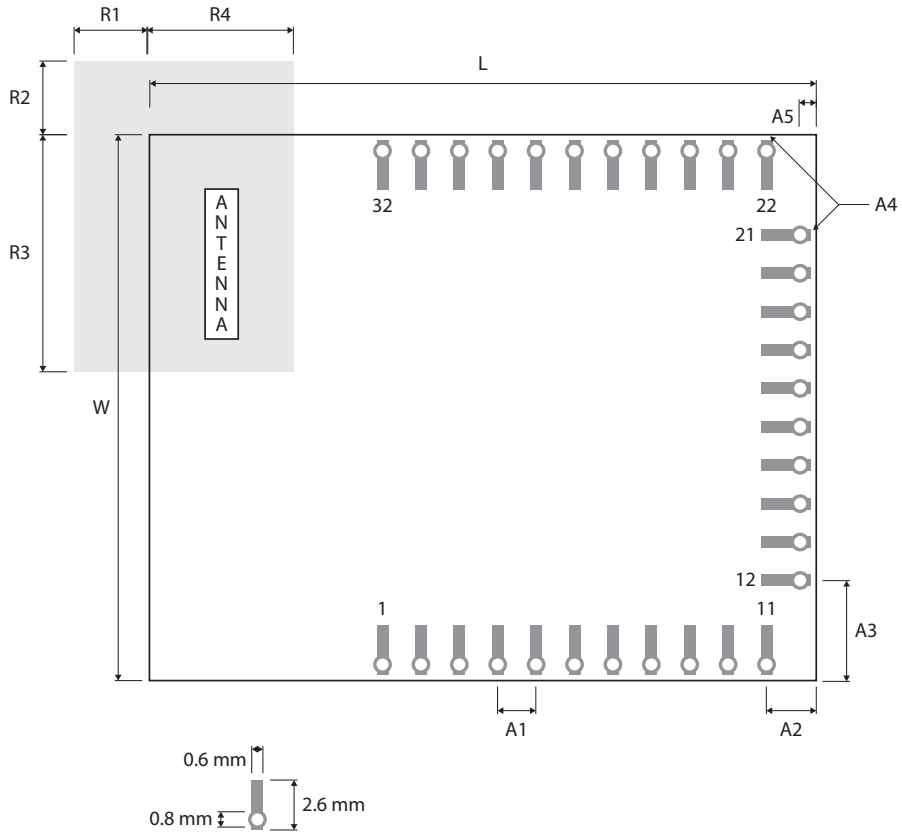
The ADC is a first-order sigma-delta converter with the following features:

- Resolution of up to 14 bits
- Sample times as fast as 5.33 µs (188 kHz)
- Differential and single-ended conversions from six external and four internal sources
- One voltage range (differential): -VREF to +VREF
- Choice of internal or external VREF
- internal VREF may be output to PB0 or external VREF may be derived from PB0
- Digital offset and gain correction
- Dedicated DMA channel with one-shot and continuous operating modes

Parameter	Min	Typical	Max	Units
Conversion time	32		4096	µs
VREF	1.17	1.2	1.23	V
VREF output current			1	mA
VREF load capacitance			10	nF
External VREF voltage range	1.1	1.2	1.3	V
External VREF input impedance	1			M Ohm
Minimum input voltage (input buffer disabled)	0			V
Minimum input voltage (input buffer enabled)	0.1			V
Maximum input voltage (input buffer disabled)			VREF	V
Maximum input voltage (input buffer enabled)			VCC – 0.1	V
Single-ended signal range (input buffer disabled)	0		VREF	V
Single-ended signal range (input buffer enabled)	0.1		VCC – 0.1	V
Differential signal range (input buffer disabled)	=-VREF		=+VREF	V
Differential signal range (input buffer enabled)	=- VCC + 0.1		+VCC – 0.1	V
Common mode range (input buffer disabled)	0		VREF	V
Common mode range (input buffer enabled)		VCC/2		V
Input referred ADC offset	-10		10	mV
Input impedance (1 MHz sample clock)	1			M Ohm
Input impedance (6 MHz sample clock)	0.5			M Ohm
Input impedance (Not Sampling)	10			M Ohm

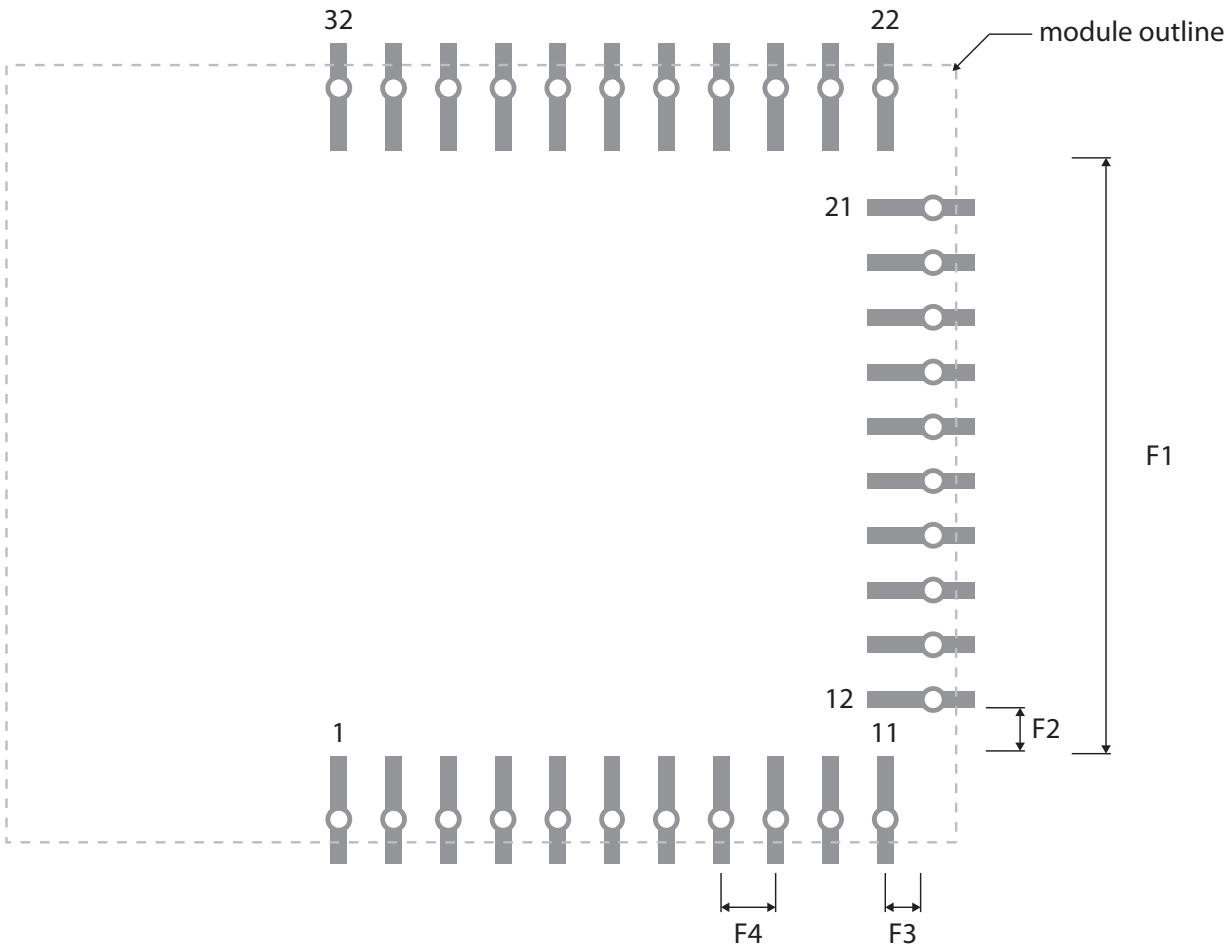
7 | Mechanical Specifications

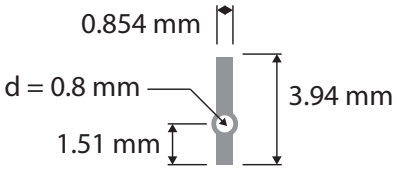
7.1 | Physical Dimensions



Symbol	Description	Distance
L	Length of the module	34.73 mm
W	Width of the module	28.43 mm
H	Height of the module	4.45 mm
A1	Pitch	2 mm
A2	Distance centre of pad to PCB edge	2.59 mm
A3	Distance center of pad to PCB edge	5.22 mm
A4	Distance pad edge to PCB edge	0.29 mm
A5	Distance center of via to PCB edge	0.84 mm
R1	Keep-out zone from corner of PCB	5 mm (minimum)
R2	Keep-out zone from corner of PCB	5 mm (minimum)
R3	Width of keep-out zone	15 mm
R4	Length of keep-out zone	5.5 mm

7.2 | Recommended Land Pattern (Surface Mount)





Symbol	Description	Distance
F1	Distance pad edge to pad edge	21.9 mm
F2	Distance pad edge to pad edge	1.523 mm
F3	Distance pad center to pad center	1.3 mm
F4	Pitch	2 mm

Note: It is advised that for surface mount applications, through holes / vias should not be designed into the carrier board.

7.3 | Connector Specifications

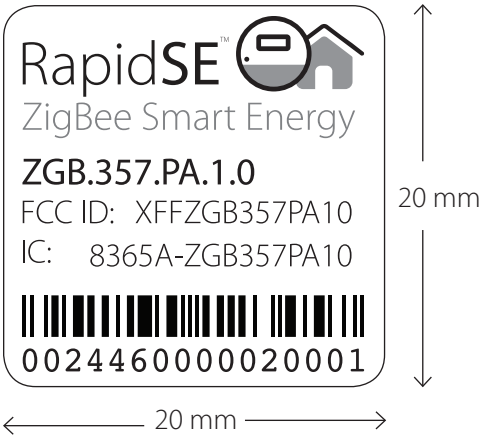
7.3.1 | Edge Mount (USNAP) Connector

10 pin 2mm pitch right angle female header

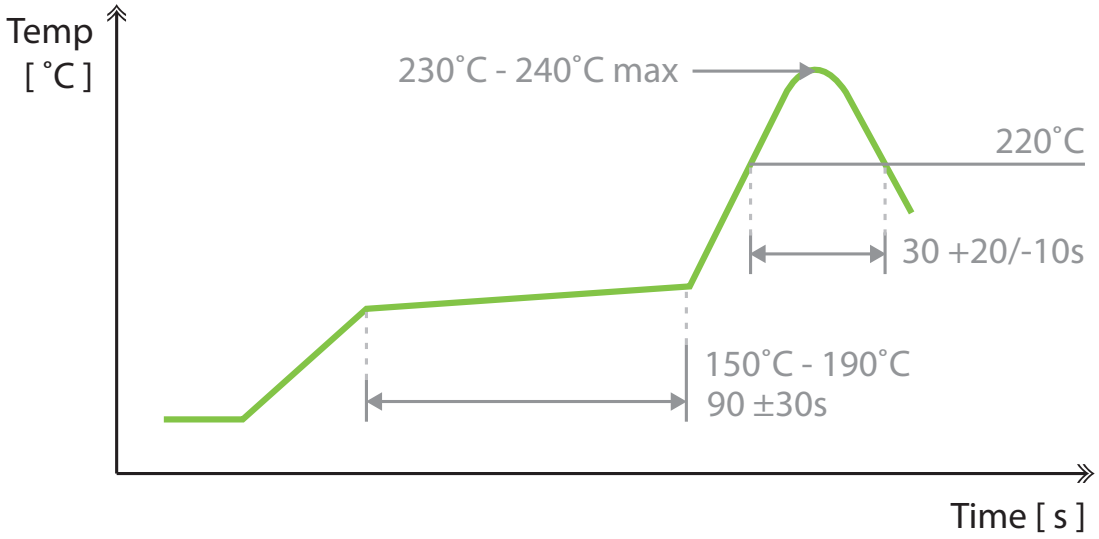
7.3.2 | SIP Header / Socket

11 + 11 + 10 (if no USNAP populated) pin 2mm pitch 0.8mm diameter through hole footprint

7.4 | Labelling



8 | **Soldering Temperature Time Profile for reflow soldering (Lead-free solder)**



Maximum reflow cycles: 2

Opposite-side reflow is prohibited due to the module weight. You must not place the module on the bottom / underside of your PCB and re-flow.

9 | Regulatory Approvals

This device comes with an onboard chip antenna. The onboard chip antenna is Johanson 2450AT43A100 while the external FCC approved antenna is Mag Layers EDA-1713-2G4C1-A2

9.1 | Federal Communications Commission (FCC - US)

9.1.1 | Approved Antennae

For the Z357PA10 module using the onboard chip antenna, the approved power level settings are 3 dBm for channels 11-25 and -10 dBm for channel 26

For the Z357PA10 module using the approved external antenna, the approved power level settings are -2 dBm for channels 11-25 and -10 dBm for channel 26

9.1.2 | FCC Notice

This device (Z357PA10-SMT, Z357PA10-USN, Z357PA10-UFL) complies with Part 15 of the FCC rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference, and
(2) This device must accept any interference received, including interference that may cause undesired operation.

To comply with FCC RF Exposure requirements, users of this device must ensure that the module be installed and/or configured to operate with a separation distance of 20cm or more from all persons.

Usage of Channel 26 at full power will result in non-compliance to FCC standards. Manufacturer recommends avoiding use of channel 26 and if necessary only use with a reduced power setting. For further details please contact Manufacturer.

9.1.3 | Modular Approval

This device (Z357PA10-SMT, Z357PA10-USN, Z357PA10-UFL) meets the requirements for modular transmitter approval as detailed in the FCC public notice DA 00-1407.
It should be noted that:

"While the applicant for a device into which an authorized module is installed is not required to obtain a new authorization for the module, this does not preclude the possibility that some other form of authorization or testing may be required for the device (e.g., a WLAN into which an authorized module is installed must still be authorized as a PC peripheral, subject to the appropriate equipment authorization)."
-- FCC Public Notice DA 00-1407

Caution:
Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

9.1.4 | Labeling Requirements

The user of this device is responsible for meeting the FCC labeling requirements. A clearly visible label on the exterior enclosure of an incorporating device must list the MMB Research Inc. FCC ID "XFFZGB357PA10" and the FCC Notice above (section 9.1.1).
Devices intended for sale in the Canadian market should also include the Industry Canada (IC) ID "8365A-ZGB357PA10".

9.2 | EU

This device is compliant with the following EU standards: ETSI EN 300 328 (v1.1.7), ETSI EN 301 489 1 (v1.8.1) and ETSI EN 301 489 17 (v2.1.1) , provided that the transmit power level is set to -7 dBm using the appropriate serial command.

10 | Ordering Information

SKU	Interface Option	Software Option	Security Certificate
Z357PA10-SMT-P-TC	Surface Mount	Pre-Programmed	Test Certificate
Z357PA10-SMT-P-PC	Surface Mount	Pre-Programmed	Production Certificate
Z357PA10-SMT-N	Surface Mount	No Software	N/A
Z357PA10-USN-P-TC	USNAP	Pre-Programmed	Test Certificate
Z357PA10-USN-P-PC	USNAP	Pre-Programmed	Production Certificate

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