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FSA9285A — MCPC-Compliant, USB-Port, Multimedia Switch with Auto-Detection, 12 V V_{BUS}

Features

Switch Type	Audio, FS/HS-USB, Charging
Switch Mechanism	Programmable Switching with Available Interrupt
Accessory Detection	Headsets with MIC and Send/End USB Data Cable USB Chargers (Car, CDP, DCP) USB On-The-Go (OTG) MCPC Specification Compliant Programmable Modes
USB	FS and HS 2.0 Compliant
USB Charging	Battery Charging 1.2 Compliant Integrated FET, Charger Detect, OCP (1.45 A), OVP (6.5 V - 14.0 V)
Audio	Left, Right, MIC (Negative Swing) Built-in Termination Resistors for Audio Pop Reduction
V_{BAT}	2.7 to 4.4 V
Programmability	I^2C
ESD	15 kV IEC 61000-4-2 Air Gap
Package	20-Lead, WLCSP (2.010 x 1.672 x 0.625 mm, 0.4 mm Pitch)
Ordering Information	FSA9285AUCX

Description

The FSA9285A is a high-performance multimedia switch featuring automatic switching and accessory detection for a USB port. The FSA9285A allows sharing of a common USB port to pass audio and USB data while simultaneously charging.

In addition, the FSA9285A integrates detection of accessories such as headphones, headsets Mobile Computing Promotion Consortium (MCPC) with MIC and Send/End, car chargers, USB chargers, USB On-The-Go (OTG), and Accessory Charging Adapters (ACA) to use a common USB connector. The FSA9285A can be programmed for manual or automatic switching of USB data paths based on the accessory detected. With an integrated 14 V over-voltage and 1.45 A over-current protected FET, the FSA9285A integrates common USB protection functions for V_{BUS}.

Applications

- Mobile Phones, Portable Media Players

Block Diagram

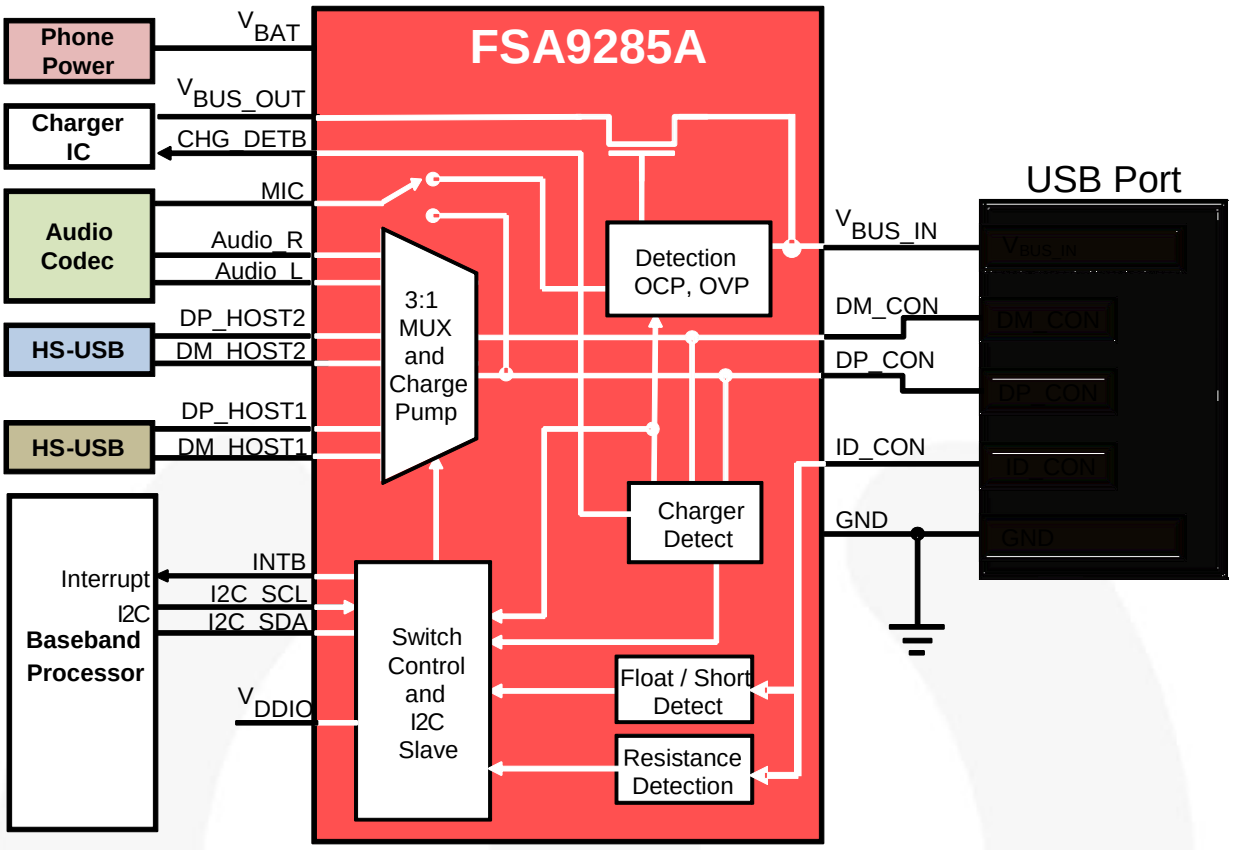


Figure 1. Block Diagram

Pin Configuration

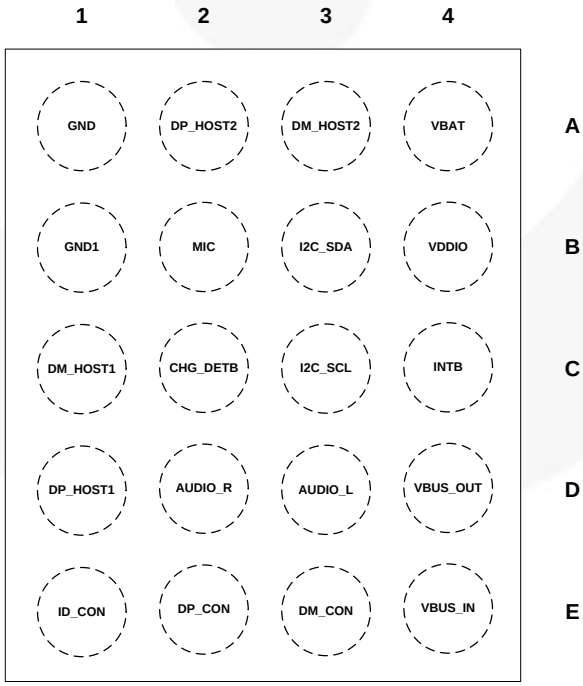


Figure 2. Pin Assignments (Top-Through View)

Pin Descriptions

Name	Pin #	Type	Default State	Description
USB Interface				
DP_HOST1	**D1**	Signal Path	Open	D+ signal switch path, dedicated USB port to be connected to the resident USB transceiver on the phone
DM_HOST1	**C1**	Signal Path	Open	D- signal switch path, dedicated USB port to be connected to the resident USB transceiver on the phone
DP_HOST2	**A2**	Signal Path	Open	D+ signal switch path, dedicated USB port to be connected to the resident USB transceiver on the phone
DM_HOST2	**A3**	Signal Path	Open	D- signal switch path, dedicated USB port to be connected to the resident USB transceiver on the phone
V_{BUS_IN}	**E4**	Power Path	N/A	Input voltage supply pin to be connected to the V_{BUS} pin of the USB connector
V_{BUS_OUT}	**D4**	Power Path	N/A	Output voltage supply pin to be connected to the source voltage pin on the charger IC
CHG_DETB	**C2**	Open-Drain Output	Hi-Z	Open-drain active LOW output, used to signal the charger IC that a charger has been attached
Audio Interface				
Audio_R	**D2**	Signal Path	Open	Right audio channel switch path from mobile phone audio CODEC
Audio_L	**D3**	Signal Path	Open	Left audio channel switch path from mobile phone audio CODEC
MIC	**B2**	Signal Path	Open	Connected to the mobile phone audio CODEC MIC input pin to complete the MIC switch path
Connector Interface				
ID_CON	**E1**	Signal Path	Open	Connected to the USB connector ID pin and used for detecting accessories or button presses
DP_CON	**E2**	Signal Path	Open	Connected to the USB connector D+ pin; depending on the signaling mode, can be switched to DP_HOST1, DP_HOST2, or Audio_R pins
DM_CON	**E3**	Signal Path	Open	Connected to the USB connector D- pin; depending on the signaling mode, can switched to DM_HOST1, DM_HOST2, or Audio_L pins
Power Interface				
V_{BAT}	**A4**	Power Path	N/A	Input voltage supply pin to be connected to the mobile phone battery output or to an internal regulator on the phone
V_{DDIO}	**B4**	Power Path	N/A	Baseband processor interface I/O supply pin
GND1	**B1**	Ground	N/A	Ground
GND	**A1**	Ground	N/A	Ground
I^2C Interface				
I2C_SCL	**C3**	Input	Hi-Z	I^2C serial clock signal to be connected to the phone-based I^2C master
I2C_SDA	**B3**	Open-Drain I/O	Hi-Z	I^2C serial data signal to be connected to the phone-based I^2C master
INTB	**C4**	CMOS Output	HIGH	Interrupt active LOW output used to prompt the phone baseband processor to read the I^2C register bits, indicates a change in ID_CON or V_{BUS_IN} pin status or accessories' attach status

1. Functional Description

The FSA9285A is a USB port accessory-detection switch with integrated 14 V over-voltage and 1.45 A over-current protected FET. Fully controlled using I^2C protocols, the FSA9285A enables all of the following to use a common connector (micro / mini USB 2.0 port): high-speed USB 2.0 standard downstream data port, stereo and mono audio headphones / headsets with or without a microphone, wired remote controller with optional send / end button, USB Charging Downstream Port (CDP) battery charger, USB Dedicated Charging Port (DCP) charger, and ANSI/CEA-936-A USB Car Kit charger.

The FSA9285A enables factory-mode testing by defaulting to manual mode (EN_MAN_SW = 1) and defaulting the MANUAL SW register to USB switches DP_HOST1 / DM_HOST1 closed and the V_{BUS} FET closed. In manual configuration, USB switches DP_HOST1 / DM_HOST1 only close when an accessory is attached that has an ID_CON resistance (ID_CON not floating) and / or valid V_{BUS} voltage is present. The V_{BUS} FET only closes when V_{BUS} is valid. All switches remain open to protect the system when there is no accessory attached. This default switch condition can be overridden with I^2C commands.

Detection of USB accessories utilizing a USB micro-B or micro-A/B connector is made possible by the presence of a standard resistor between the ID pin and ground of the accessory. Advanced modes manage wired remote-control sensing for audio accessories. The FSA9285A is designed to allow audio signals to swing below ground on the USB 2.0 port data lines. Internal power for the FSA9285A is automatically derived from either the battery voltage (V_{BAT}) or the USB supply (V_{BUS_IN}) for simplicity and long battery life.

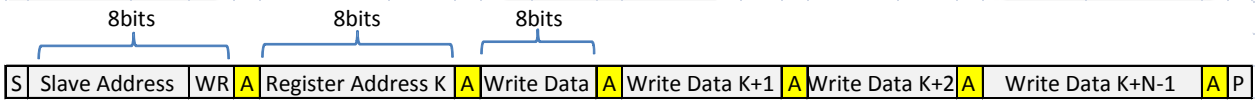
2. I^2C and Digital Core

The FSA9285A includes a full I^2C slave controller. The I^2C slave fully complies with version 2.1 of the I^2C specifications. This block is designed for fast-mode, 400 kHz signals. The slave addresses are shown in Table 1. This block also includes the chip master controller. The chip controller monitors commands sent to the FSA9285A via I^2C from the baseband processor and takes action. The digital core takes inputs from the various functional blocks and the I^2C commands received from the mobile phone baseband processor and relays relevant status updates to the phone.

Table 1. I^2C Slave Address

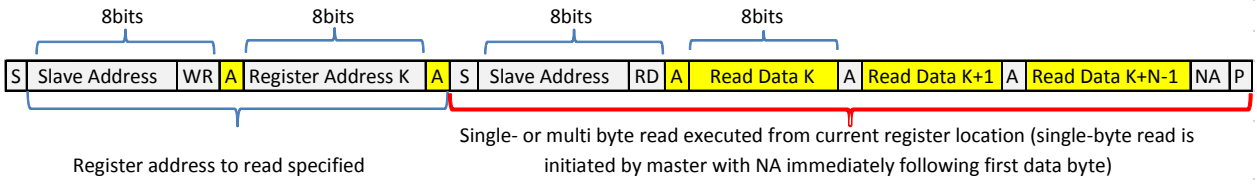
Name	Size (Bits)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Slave Address	8	0	1	0	0	1	0	1	Read / Write

Examples of I^2C write and read sequences are shown in Figure 3 and Figure 4, respectively.



Note: Single byte read is initiated by master with P immediately following first data byte.

Figure 3. I^2C Write Sequence



Note: If register is not specified, master begins reading from current register. In this case, only red bracketed sequence is needed.

Figure 4. I^2C Read Sequence

From Master to Slave
From Slave to Master

S Start Condition
A Acknowledge (SDA Low)
NA NOT Acknowledge (SDA High)
WR Write=0
RD Read =1
P Stop Condition

3. Power-Up Initialization and Reset

FSA9285A operates correctly without special power sequencing. When power is first applied, the device undergoes a hardware reset and all the registers are initialized to the default values shown in Table 6. All of the combinations of valid V_{BUS_IN} and V_{BAT} are shown in Table 2.

As shown in Table 2, V_{BAT} is used as the primary power supply. V_{DDIO} is the dedicated baseband IO voltage and is only used for I^2C interface and interrupt processing within the FSA9285A.

When V_{BAT} is not valid, but V_{BUS_IN} is; the FSA9285A powers off V_{BUS_IN}. In this condition, the FSA9285A operates in its default state and is able to detect USB accessories and all chargers. The FSA9285A always turns on the V_{BUS} FET upon any attach state with V_{BUS_Valid} (unless Manual Mode is enabled with the V_{BUS} FET switch state configured open). This allows charging of a dead battery when the rest of the system is not powered to configure the FSA9285A.

When the device is reset, all I^2C registers are initialized to the default values shown in Table 6 *(see Section 4 - Configuration)*. After reset or power up, the FSA9285A enters Standby Mode and is ready to detect accessories sensed on its V_{BUS_IN} or ID_CON pins.

The device has three hardware reset mechanisms:

- Power-on reset caused by the initial rising edge of V_{BUS} (if V_{BAT} < 1.0 V) or rising edge of V_{BAT} (If not V_{BUS_VALID})
- The falling edge of V_{DDIO}
- I^2C reset: holding I2C_SDA and I2C_SCL LOW for 30 ms

The device has one software reset mechanism:

- Writing the ResetB bit (bit 6) in the Control register (02h)

Table 2. Power States Summary

Valid V_{BUS_IN}	Valid V_{BAT}	Valid V_{DDIO} (1)	Power State	Enabled Functionality		
				Charging through FET	Processor Communication (I^2C & Interrupts)	Detection
NO	NO	NO	Power Down	NO	NO	NO
NO	NO	YES (2)		ILLEGAL STATE		
NO	YES	NO	Powered Off V_{BAT}	NO	NO	YES
NO	YES	YES	Powered Off V_{BAT}	NO	YES	YES
YES	NO	NO	Powered Off V_{BUS_IN}	Yes	NO	YES
YES	YES	NO	Powered Off V_{BAT}	YES	NO	YES
YES	NO	YES (2)	Powered Off V_{BUS_IN}	YES	YES	YES
YES	YES	YES	Powered Off V_{BAT}	YES	YES	YES

Notes:
1. V_{DDIO} is expected to be the same supply used by the baseband I/Os.
2. This is not a typical state. Both V_{BAT} and V_{DDIO} are typically provided from the same regulator.

4. Configuration

The FSA9285A must be configured for operation upon reset. There are several options to note about reset configuration:

1. The Interrupt Mask bit is set and must be cleared for the FSA9285A to interrupt the host processor.
2. Upon hardware reset, the USB Path DP_HOST1 / DM_HOST1 switches are configured to close when an accessory is attached (with an ID_CON resistance or valid V_{BUS} voltage) to support production programming. These switches may be opened using I^2C commands.
3. If MIC Mode is going to be used, it is recommended that MIC_OVP_EN bit be set to 1 at reset.
4. To enable manual configuration of the USB switches, the EN_MAN_SW bit must be set to 1. The switch settings then override any automatic settings (this assumes that the USB discovery state machine has completed its operations and a device is attached). For the weak (or dead) battery case to work reliably, V_{DDIO} must be removed (to reset the FSA9285A state) whenever the battery is too low for reliable I^2C communication.
5. Performing a software reset sets all I^2C Register Map (Table 6) registers to default, with the exception of the Control register, Manual SW register, and the Manual CHG_CTRL register. These registers are only reset to default on a hardware reset.

5. Interrupt Operation

The baseband processor recognizes interrupt signals by observing the INTB signal, which is active LOW. Interrupts are masked upon reset via the INT Mask register bit (bit 0 of Control register, address 02h in Table 6 of the I^2C register map) and INTB pin defaults HIGH. After the INT Mask bit is cleared by the baseband processor, the INTB pin is generally driven HIGH (INTB is not an open-drain output) in preparation for a future interrupt. The INTB remains HIGH until the INTB mask is cleared. If the Interrupt Mask bit in the I^2C Control register is written LOW when an interruptible event occurs, INTB transitions LOW and returns HIGH when the processor reads the Interrupt register at addresses 03h.

6. Analog Switch Descriptions

The FSA9285A has a three-port data switch, providing routing capability to two data ports and one audio port. The two data switches are high bandwidth to provide high-speed USB 2.0 “eye” compliance. These switches also operate full-swing for full-speed USB and UART signals up to 4.4 V.

The high-performance negative-swing-capable audio switch utilizes a termination resistor for audio pop reduction. The audio configuration also provides for routing a microphone signal from a headset. The MIC signals can be routed to either the V_{BUS_IN} pin for stereo audio configurations or the DP_CON pin for mono audio configurations that also allow simultaneous charging over the V_{BUS} line.

7. Accessory Detection

In Standby Mode, after power-up or reset, the FSA9285A monitors the V_{BUS_IN} and ID_CON pins for any connectivity using very low power (*see “Battery Supply Standby Mode Current” in the Switch Path DC Electrical Characteristics section)*. To minimize standby power, many functional blocks are powered down until an accessory attach is detected. The V_{BUS_IN} detection recognizes if the voltage on V_{BUS_IN} is within the valid range (>4.0 V). For resistance to GND on the ID_CON pin, the FSA9285A measures voltage with an injected current to determine this resistance. All accessories attached or detached are reported to the processor via the Interrupt register. Any changes of resistance on the ID_CON pin are reported as a Resistor_Change interrupt. Additional information about the accessory is reported in the Device Type, Resistor Code, and Status registers. For USB accessories without an ID_CON resistance, a V_{BUS_Valid} Change interrupt is reported to signal an attach or detach condition. Status of V_{BUS_Valid} and ID_CON resistance is always available after any interrupt.

The USB detection flow is show in Figure 5. Note that the INTB Mask bit in the Control register must be cleared after a reset or power-up before interrupts can be signaled by the FSA9285A. Individual Interrupt Masks bits can be enabled by writing the Interrupt Mask register *(see Table 6)*.

ID_CON resistor detection is accomplished in a little more than three times the “Resistor Detection Time,” where Resistor Detection Time bits are programmable in the Timing Set register. The FSA9285A is designed to allow up to 1 nF capacitance on the ID_CON pin. ID_CON is short-circuit protected from a faulty resistor or an accidental short where the current is limited to 5 mA sourced by the FSA9285A.

The detection of a V_{BUS_IN} goes through the USB detection flow only once. V_{BUS_IN} must be removed before the USB detection state machine reverts to its initial state.

After an initial attach, the FSA9285A continuously monitors the ID pin for changes and reports those changes to the baseband processor. To provide the fastest response for changes in button checking after initial attach, the FSA9285A indicates a change in ID_CON resistor after two samples are taken instead of the three consecutive samples taken on initial attach. To save power, the resistor detection block can be disabled after an initial attach with the ID_DIS bit in the Control register. The resistor detection block is normally disabled when no ID_CON resistance is present (ID_CON floating) to save power. The condition of ID_FLOAT continues to be monitored regardless of the ID_DIS setting.

Whenever a resistance is measured on ID_CON, the USB discovery state machine halts after completion of its current state and the ID_CON state machine continues for accessory detection. The only exception is when an ACA RID-A accessory is detected. In this case, the USB discovery state machine is used to differentiate between a docking station and a powered A-device attached to a docking station *(per USB Battery Charging Specification 1.2)*.

If the EN_MAN_SW bit is set on attach, FSA9285A configures the switches to the state in the MANUAL SW register.

Upon the removal of any accessory, the FSA9285A detects and indicates a change in ID_CON resistance (regardless of ID_DIS bit setting), a removal of V_{BUS_IN}, or both. The FSA9285A automatically opens all switches (and V_{BUS} FET) on detach (ID_FLOAT and V_{BUS} not valid), even if the FSA9285A is set to Manual Switching Mode.

For the weak battery case, the FSA9285A needs to be in Automatic Switching Mode. Should the processor NOT be able to respond to INTB, FSA9285A must be placed in Automatic Switching Mode explicitly or V_{DDIO} must be removed, resetting the FSA9285A state to its default values.

Note: If the FSA9285A is to be used in automatic switching mode (EN_MAN_SW = 0) then the Manual SW register must be configured for all switches OPEN).

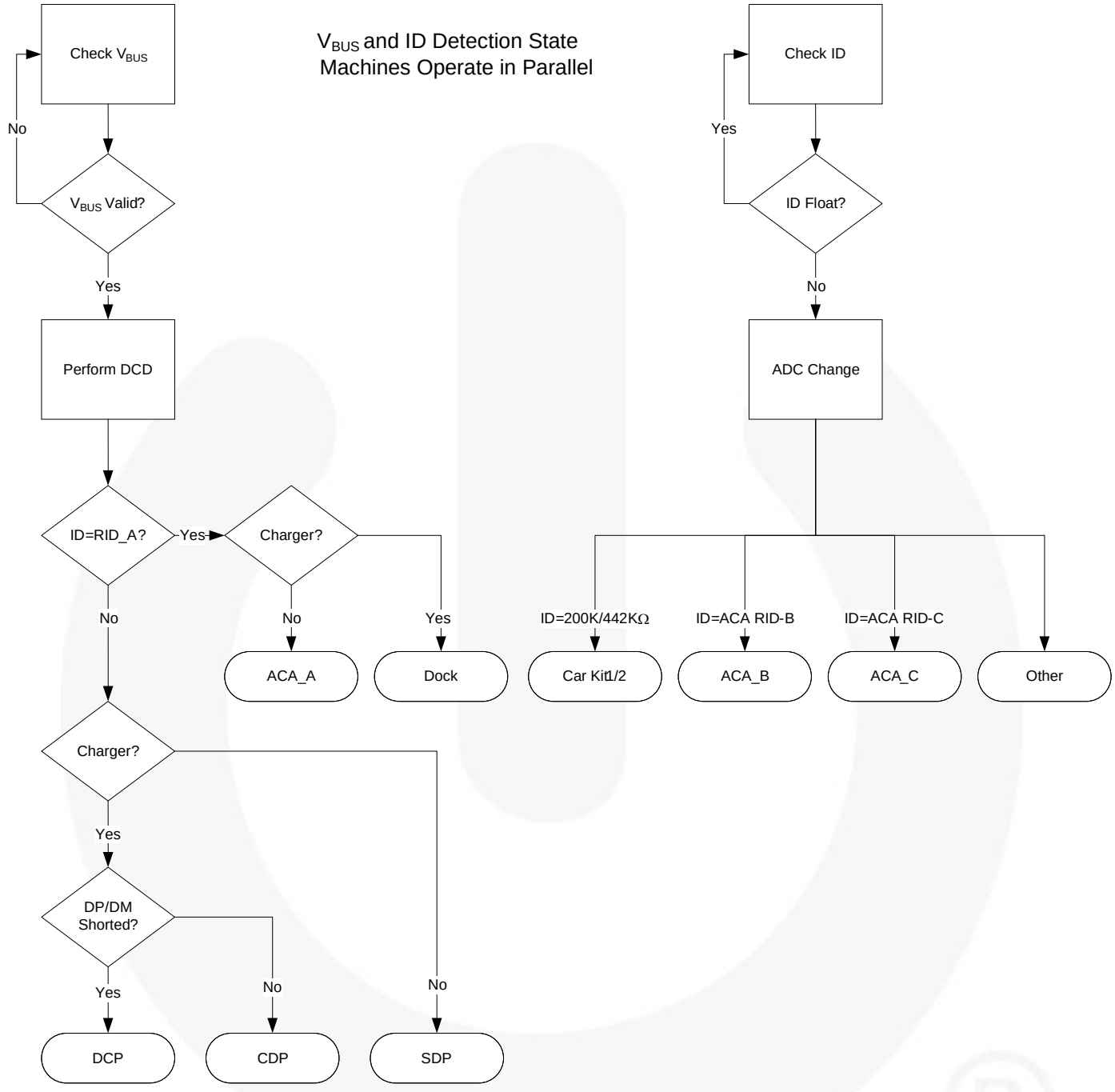


Figure 5. Accessory Discovery State Machine Flow Diagram

Note:

3. Figure 5 illustrates operation with a valid V_{DDIO} supply voltage. Figure 5 does not illustrate Dead Battery Provision (DBP) *See Section 9 for details*.

Table 3. ID_CON Resistor Identification

Resistor Code[4]	ID_CON Resistance to GND			Auto Switch USB Switches	Unit	Accessory Detected
	Min.	Typ.	Max.			
10110	0		18		Ω	OTG
10100	19000	20000	21000		Ω	Resistor 20 kΩ
10011	22800	24000	25200		Ω	Resistor 24 kΩ
10010	27265	28700	30135		Ω	Resistor 28.7 kΩ
10001	34675	36500	36865	YES	Ω	ACA RID-C[5]
10000	39798	40200	40602		Ω	Resistor 40.2 kΩ
01111	44650	47000	49350		Ω	MCPC Send/End
01110	55638	56200	56762		Ω	Resistor 56.2 kΩ
01101	64600	68000	71400	YES	Ω	ACA RID-B[5]
01100	80275	84500	88725		Ω	Resistor 84.5 kΩ
01011	96900	102000	107100		Ω	Phone Power Device
01010	117800	124000	130200	YES	Ω	ACA RID-A[5]
01001	148500	150000	151500		Ω	Resistor 150 kΩ
01000	171000	180000	183600		Ω	MCPC Maintenance
00111	198000	200000	202000		Ω	Car Kit Type-1 Charger[5]
00110	229680	232000	234320		Ω	Resistor 232 kΩ
00101	272650	287000	301350		Ω	MCPC Mode 1
00100	370500	390000	401700		Ω	MCPC Reserved
00011	437580	442000	446420		Ω	Car Kit Type-2 Charger[5]
00010	529150	557000	584850		Ω	MCPC Mode 3
00001	757150	797000	836850		Ω	MCPC Mode 2
00000	970000		Open		Ω	Float[6]

Notes:

4. The resistor code values are reported in the Resistor Code register whenever a valid resistor code value changes.
5. *See Table 4 for details, additional requirements may be applicable for detection*.
6. Resistance ≥ 970 kΩ status bit /ID_FLOAT=0.

8. USB Port and Charger Detection

The FSA9285A can detect the USB 2.0 port types summarized in Table 4. V_{BUS} must be present to detect these accessories.

For SDP, CDP, and ACA USB accessories; the following pin mapping is automatically configured:

- DP_HOST1 = DP_CON (If EN_MAN_SW = 0)
- DM_HOST1 = DM_CON (If EN_MAN_SW = 0)
- $V_{BUS\_OUT} = V_{BUS\_IN}$

The FSA9285A allows factory testing or programming through the DP_HOST1 and DM_HOST1 switches by closing these switches when a USB cable with an ID resistance or V_{BUS} voltage is detected.

For USB chargers that do not automatically close USB switches, the switches can be closed manually through the Manual Switch register when EN_MAN_SW is enabled.

Whenever V_{BUS_IN} becomes valid, the integrated charger FET is closed (unless EN_MAN_SW = 1 and Manual SW[1:0]≠11) and V_{BUS_IN} voltage is continuously monitored to incorporate Over-Voltage Protection (OVP). If the attached device is recognized as one of the chargers in Table 4 (excluding SDP), the CHG_DETB pin goes LOW to send a signal to the charger IC, external to the FSA9285A, to increase the charging current to the maximum allowed level by the Over-Current Protection (OCP) trigger *(see the Switch Path DC Electrical Characteristics section)*. V_{BUS_OUT} must be valid 10 ms before sourcing greater than 100 mA.

Table 4. ID_CON and V_{BUS} Detection for USB and Car Kit Devices

Resistor Code[7]	V_{BUS_IN}	USB Switches[8]	CHG_DETB[8]	ID_CON Resistance to GND			Accessory Detected
				Min.	Typ.	Max.	
00111	5 V	Open	Asserted	198 kΩ	200 kΩ	202 kΩ	Car Kit Type-1 Charger
00011	5 V	Open	Asserted	437.58 kΩ	442 kΩ	446.42 kΩ	Car Kit Type-2 Charger
00000	5 V	Open	Asserted	3 MΩ	Open	Open	USB Dedicated Charging Port, Travel Adapter or Dedicated Charger (DCP)[9]
00000	5 V	Auto_close	Asserted	3 MΩ	Open	Open	USB Charging Downstream Port (CDP)[9]
00000	5 V	Auto_close	Not Asserted	3 MΩ	Open	Open	USB Standard Downstream Port (SDP)[9]
10001	5 V	Auto_close	Asserted	34.675 kΩ	36.5 kΩ	36.865 kΩ	ACA RID-C
01101	5 V	Auto_close	Asserted	64.6 kΩ	68 kΩ	71.4 kΩ	ACA RID-B
01010	5 V	Auto_close	Asserted	117.8 kΩ	124 kΩ	130.2 kΩ	ACA RID-A

Notes:
7. The resistor code values are reported in the Resistor Code register, independent of the state of USB switches or V_{BUS_IN}.
8. In Table 4, switches auto-close and CHG_DETB are asserted only if V_{BUS_VALID}.
9. The FSA9285A follows the Battery Charging 1.2 specification, which uses DP_CON and DM_CON to determine the USB accessory attached. *Refer to Battery Charging 1.2 Specification for details.*

9. Dead Battery Provision

Since V_{BUS} charging power connects through it, the FSA9285A must automatically turn on the V_{BUS} FET to allow the mobile device to charge after shutdown due to a dead battery. When detecting that V_{BUS} is valid, the FSA9285A automatically turns on the V_{BUS} FET after BC1.2 charger detection is complete. Turning on at this time allows the DP / DM switches to turn on at the same time as the V_{BUS} FET.

If the FSA9285A detects a USB port (SDP, CDP, or DCP) when V_{BAT} and V_{DDIO} are not valid, it applies 0.6 V to DP_CON in accordance with the USB BC1.2 Dead Battery Provision. The FSA9285A automatically removes the 0.6 V on DP_CON upon detach of an accessory, when V_{DDIO} returns to a valid voltage, or when $V_{BAT} > V_{BAT\_TH}$. If the mobile device should manually assert the 0.6 V on DP_CON, it can do so using the ASSERT_D+ bit (bit 2) of the Manual CHG_CTRL register (14h); V_{BUS} must be valid to do so.

10. Over-Voltage Protection (OVP) and Over-Current Protection (OCP)

When V_{BUS_IN} is less than nominally 6.5 V, the FSA9285A allows the V_{BUS_IN} supply to enter the chip-power select voltage regulator block. For V_{BUS_IN} greater than nominally 6.5 V, the input is disconnected, protecting the FSA9285A from excess voltage. Upon entering Shutdown Mode, the OVP bit in the Interrupt register is set HIGH (to reflect a change in OVP state) and an interrupt is sent to the baseband. The OVP Status register is also written HIGH to indicate that an OVP condition is present. In Shutdown Mode, the FSA9285A continually monitors V_{BUS} and exits Shutdown Mode when V_{BUS} drops to below 6.5 V or it senses an accessory detach. Upon exiting an OVP condition, another OVP interrupt is triggered (reflecting a change in OVP state) and the OVP status bit is cleared (indicating an OVP condition is not present).

The Over-Current Protection (OCP) feature limits current through the charger FET to nominally 1.45 A. OCP is only implemented when V_{BUS_IN} is provided by the attached accessory. The FSA9285A senses an over-current event, opens (turns off) the V_{BUS} FET, and reports this to the baseband by asserting the OCP bit (to reflect a change in OCP state) in the Interrupt register. When in an OCP state, the OCP status bit is written HIGH. While the OCP condition is present, the FSA9285A continually monitors the V_{BUS} current and exits Shutdown Mode when the V_{BUS} current drops below nominally 1.45 A or it senses an accessory detach. Upon exiting OCP state, the OCP Interrupt bit is again written HIGH, indicating a change in OCP state and the OCP Status bit is written LOW, indicating an OCP state is not present.

11. Audio Accessory Detection

After an audio device is attached and a change in ID_CON resistance is detected (if ID_DIS=0), the FSA9285A asserts an interrupt and the baseband processor can read the Resistor Code register to determine the ID_CON resistance change to detect if a key, such as MCPC SEND / END, was pressed.

For powered audio accessories with V_{BUS} present, the FSA9285A detects when V_{BUS} is valid and interrupts the baseband processor. The baseband processor must manually control the FSA9285A switches for proper functionality. MIC can be switched to either V_{BUS} or DP_CON through the Manual SW register, allowing more flexibility.

12. Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter			Min.	Max.	Unit
V_{BAT}/V_{DDIO}	Supply Voltage from Battery / Baseband			-0.5	6.0	V
V_{BUS_IN}	Supply Voltage from Micro-USB Connector			-0.5	28.0	V
V_{SW}	Switch I/O Voltage	USB		-1.0	6.0	V
		Stereo/Mono Audio Path Active		-2.0	6.0	
		All Other Channels		-0.5	6.0	
I_{IK}	Input Clamp Diode Current			-50		mA
I_{CHG}	Charger Detect CHG_DETB Pin Current Sink Capability				30	mA
I_{SW}	Switch I/O Current (Continuous)	USB			50	mA
		Audio			60	
		All Other Channels			50	
I_{SWPEAK}	Peak Switch Current (Pulsed at 1 ms Duration, <10% Duty Cycle)	USB			150	mA
		Audio			150	mA
		Charger FET			2	A
		All Other Channels			150	mA
T_{STG}	Storage Temperature Range			-65	+150	°C
T_J	Maximum Junction Temperature				+150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)				+260	°C
ESD	IEC 61000-4-2 System Level	USB Connector Pins (DP_CON, DM_CON, V_{BUS_IN}, ID_CON) to GND	Air Gap	15000		V
			Contact	8000		
	Human Body Model, JEDEC JESD22-A114		All Pins	5000		
	Charged Device Model, JEDEC JESD22-C101		All Pins	1500		

13. Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{BAT}	Battery Supply Voltage		2.7	3.8	4.4	V
V_{BAT_TH}	Battery Supply Voltage Threshold for Weak / Dead Battery		2.7	3.0	3.3	V
V_{BUS_IN}	Supply Voltage from V_{BUS_IN} Pin		4.0		14.0[10]	V
V_{DDIO}	Processor Supply Voltage		1.7		3.6	V
V_{SW}	Switch I/O Voltage	USB Path Active	0		4.4	V
		Audio Path Active	-1.5		3.0	
		All Other Pins	0		5.0	
ID_{CAP}	Capacitive Load on ID_CON Pin for Reliable Accessory Detection				1.0	nF
T_A	Operating Temperature		-40		+85	ºC

Note:

10. Maximum operating condition set by design.

14. Switch Path DC Electrical Characteristics

All typical values are at T_A=25°C unless otherwise specified.

Symbol	Parameter	V_{BAT} (V)	Condition	T_A = -40 to +85°C			Unit
				Min.	Typ.	Max.	
Host Interface Pins (INTB, CHG-DETB)							
V_{OH}	Output High Voltage(11)	3.0 to 4.4	I_{OH}=2 mA	0.7 x V_{DDIO}			V
V_{OL}	Output Low Voltage	3.0 to 4.4	I_{OL}=8 mA			0.4	V
I^2C Interface Pins – Fast Mode (I2C_SDA, I2C_SCL)							
V_{IL}	Low-Level Input Voltage	3.0 to 4.4				0.3 x V_{DDIO}	V
V_{IH}	High-Level Input Voltage	3.0 to 4.4		0.7 x V_{DDIO}			V
I_{I2C}	Input Current of I2C_SDA and I2C_SCL Pins, Input Voltage 0.26 V to 2.34 V	3.0 to 4.4		-10		10	µA
Switch Off Characteristics							
I_{OFF}	Power-Off Leakage Current	0	All Data Ports Except Audio & MIC, V_{SW}=4.4 V			10	µA
$I_{NO(OFF)}$	Off Leakage Current	4.4	All Ports Except Audio & MIC, I/O Pins=0.3 V, 4.1 V, or Floating	-0.100	0.001	0.100	µA
I_{IDSHRT}	Short-Circuit Current	3.0 to 4.4	Current Limit if ID_CON=0		5		mA
USB Switch (DP_HOSTn, DM_HOSTn) ON Paths							
R_{ON}	USB Switch Paths On Resistance(12,13)	3.0 to 4.4	$V_{D+/D-}$=0, 0.4 V, I_{ON}=8 mA		8	10	Ω
			$V_{D+/D-}$=0, 3.6 V, I_{ON}=8 mA		11	17	Ω
Charging FET ON Path							
V_{OVP}	Over-Voltage Protection (OVP) Threshold Voltage	3.0 to 4.4		6.2	6.5	6.9	V
R_{ON}	Charging FET On Resistance(12,13)	3.0 to 4.4	V_{BUS_IN}=4.2 V-5.0 V, I_{ON}=1 A		200		mΩ
I_{OCP}	Over-Current Protection (OCP) Threshold Current	3.0 to 4.4	V_{BUS_IN}=5.2 V	1.20		1.65	A

Continued on the following page…

Switch Path DC Electrical Characteristics (Continued)

All typical values are at T_A=25°C unless otherwise specified.

Symbol	Parameter	V_{BAT} (V)	V_{BUS}(V)	Condition	T_A = -40 to +85°C			Unit
					Min.	Typ.	Max.	
Audio_R / Audio_L Switch ON Paths								
R_{ON}	Audio Switch On Resistance[12,13]	3.0 to 4.4		$V_{L/R}$=-0.8 V, 0.8 V; I_{ON}=30 mA; f=0-470 kHz			3.5	Ω
				$V_{L/R}$=-1.5 V, 1.5 V; I_{ON}=30 mA, f=0-470 kHz			4.0	
R_{FLAT}	Audio R_{ON} Flatness[12,14]	3.0 to 4.4		$V_{L/R}$=-0.8 V, 0.8 V; I_{ON}=30 mA, f=0-470 kHz			0.1	Ω
				$V_{L/R}$=-1.5 V, 1.5 V; I_{ON}=30 mA, f=0-470 kHz			0.2	
R_{TERM}	Internal Termination Resistors					1.5		kΩ
MIC Switch ON Paths								
R_{ON}	MIC Path ON Resistance[12,13]	3.0 to 4.4		MIC Connected to V_{BUS_IN}, V_{SW}=0, 2.8 V; I_{ON}=30 mA		40		Ω
				MIC Connected to DP_CON, V_{SW}=0, 2.8 V; I_{ON}=30 mA		40		
MIC_{OVP}	Over-Voltage Protection (OVP) Threshold Voltage with MIC on V_{BUS_IN}[15]			MIC Connected to V_{BUS_IN} Entering OVP	2.80		3.35	V
Total Current Consumption[17]								
I_{BAT}	Battery Supply Standby Mode Current No Accessory Attached (ID_CON Floating)	3.0 to 4.4	Floating	VBUS Floating		10	15	µA
	Average Battery Supply Standby Mode Current with Accessory Attached (ID_CON Not Floating)		0.0	ID_DIS=1		35	50	
			5.0	ID_DIS=1		100[16]	150[16]	

Notes:

11. Does not apply to the CHG_DETB pin because it is open drain.
12. Limits based on Electrical Characterization data.
13. On resistance is the voltage drop between the two terminals at the indicated current through the switch.
14. Flatness is the difference between the maximum and minimum values of on resistance over the specified range of conditions.
15. The MIC bias applied should not exceed 2.8 V.
16. V_{DDIO} of either 0 V or in the valid range of 1.7 V to 3.6 V.
17. Typically the battery charges from V_{BUS}.

15. Capacitance

Symbol	Parameter	V_{BAT} (V)	Condition	T_A = -40 to +85°C			Unit
				Min.	Typ.	Max.	
C_{ONUSB}	DP_CON, DM_CON On Capacitance (USB Mode, Both HOST1 and HOST2)	3.8	V_{BIAS}=0.2 V, f=1 MHz		8		pF
C_I	Capacitance for Each I/O Pin	3.8			2		pF
C_{OFF}	Off Capacitance (HOST1 and HOST2)	3.8			2		pF

16. I²C AC Electrical Characteristics

Symbol	Parameter	Fast Mode		
		Min.	Max.	Unit
f_{SCL}	SCL Clock Frequency	0	400	kHz
$t_{HD;STA}$	Hold Time (Repeated) START Condition	0.6		µs
t_{LOW}	LOW Period of SCL Clock	1.3		µs
t_{HIGH}	HIGH Period of SCL Clock	0.6		µs
$t_{SU;STA}$	Set-up Time for Repeated START Condition	0.6		µs
$t_{HD;DAT}$	Data Hold Time	0	0.9	µs
$t_{SU;DAT}$	Data Set-up Time(18)	100		ns
t_r	Rise Time of SDA and SCL Signals(19)	20+0.1C_b(18)	300	ns
t_f	Fall Time of SDA and SCL Signals(19)	20+0.1C_b(18)	300	ns
$t_{SU;STO}$	Set-up Time for STOP Condition	0.6		µs
t_{BUF}	BUS-Free Time between STOP and START Conditions	1.3		µs
t_{SP}	Pulse Width of Spikes that Must Be Suppressed by the Input Filter	0	50	ns

Notes:

18. C_b equals the total capacitance of one BUS line in pf. If mixed with high-speed devices; faster fall times are allowed, according to the I²C Bus specification.
19. A fast-mode I²C Bus® device can be used in a Standard-Mode I²C-Bus system, but the requirement that $t_{SU;DAT} \geq 250$ ns must be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r\_max} + t_{SU;DAT} = 1000 + 250 = 1250$ ns before the SCL line is released (according to the Standard-Mode I²C Bus specification).

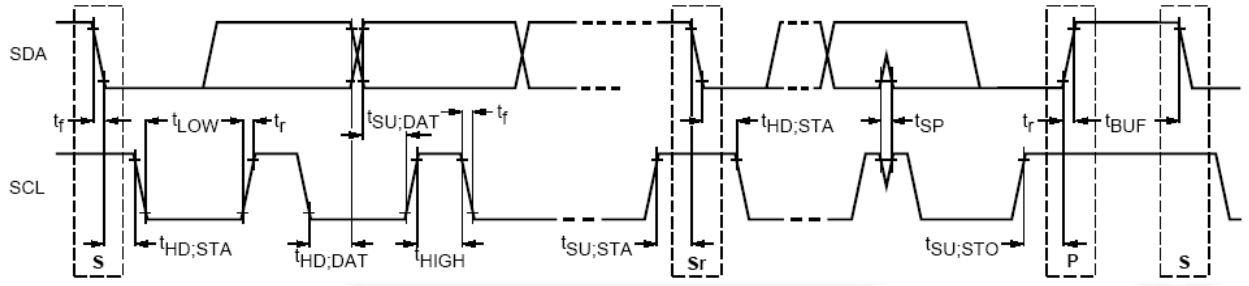


Figure 6. Definition of Timing for Full-Speed Mode Devices on the I²C Bus®

Table 5. I²C Slave Address

Name	Size (Bits)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Slave Address	8	0	1	0	0	1	0	1	R/W

17. Switch Path AC Electrical Characteristics

All typical values are for V_{BAT}=3.8 V at T_A=25ºC unless otherwise specified.

Symbol	Parameter		Conditions	T_A = -40 to +85°C			Unit
				Min.	Typ.	Max.	
Xtalk	Active Channel Crosstalk DP_CON to DM_CON	Audio Mode	f=20 kHz, R_T=32 Ω, C_L=0 pF		-90		dB
		USB Mode	f=1 MHz, R_T=50 Ω, C_L=0 pF		-60		
O_{IRR}	Off Isolation	Audio Mode	f=20 kHz, R_T=32 Ω, C_L=0 pF		-100		dB
		USB Mode	f=1 MHz, R_T=50 Ω, C_L=0 pF		-60		
PSRR	Power Supply Rejection Ratio, MIC on V_{BUS_IN}		Power Supply Noise 300 Mv_{PP}, f=217 Hz Sine Wave		-100		dB
THD	Total Harmonic Distortion (Audio Path)		20 Hz to 20 kHz, R_L=32/16 Ω, Input Signal Range -1.5 V, +1.5 V		0.07		%
$t_{SK(P)}$	Skew of Opposite Transitions of the Same Output (USB Mode)		t_r=t_f=750 ps (10-90%) at 240 MHz, C_L=0 pF, R_L=50 Ω		35		ps
t_{I2CRST}	Time When I2C_SDA and I2C_SCL Both LOW to Cause Reset		*See Figure 7*	30			ms
t_{SDPDET}	Time from V_{BUS_IN} Valid to V_{BUS_OUT} Valid with Charger FET Closed and USB Switches Closed for USB Standard Downstream Port		*See Figure 9*		120		ms
t_{CHGOUT}	Time from V_{BUS_IN} Valid to V_{BUS_OUT} Valid with Charger FET Closed for Both USB Charging Ports (CDP and DCP)		*See Figure 10*		160		ms
t_{CARKIT}	Time from V_{BUS_IN} Valid to Car Kit Type-1 or Type-2 Charger Detected		*See Figure 11*		140		ms
t_{IDDET}	Time from ID_CON Not Floating to INTB LOW to Signal Accessory Attached that is ID_CON Resistance-Based Only (V_{BUS_IN} Not Valid, Default timing configuration)		*See Figure 12*		150		ms
t_{BC11}	Timeout for Data Contact During DCD Check			300	600	900	ms

18. Timing Diagrams

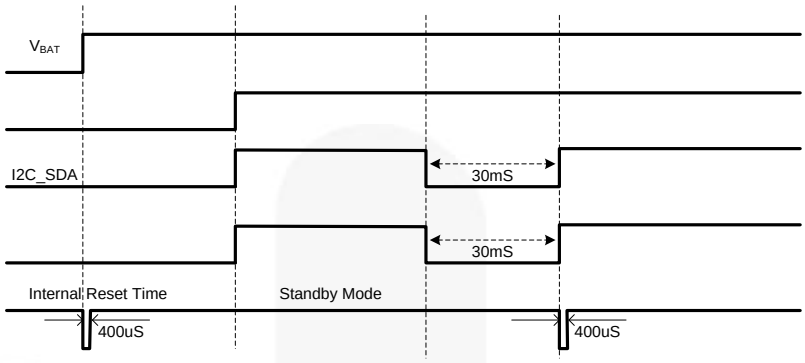


Figure 7. I^2C Reset Mode Timing

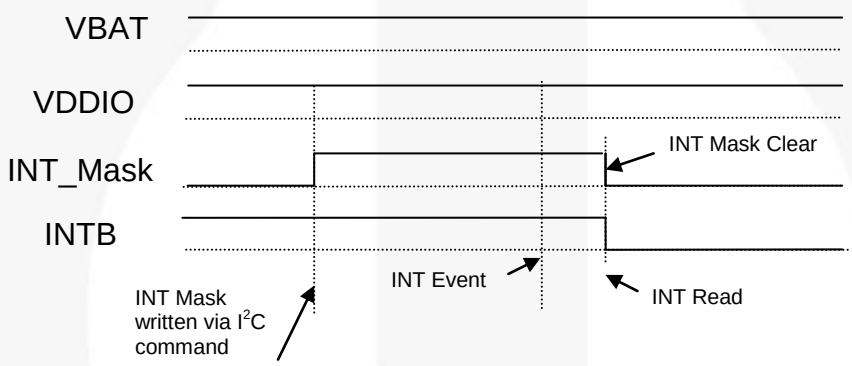


Figure 8. INT Mask to INTB Interrupt Timing Diagram

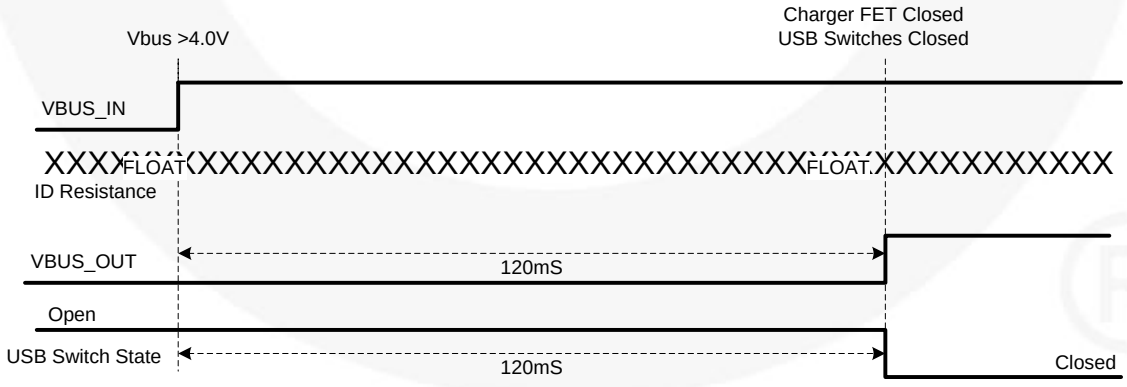


Figure 9. USB Standard Downstream Port Attach Timing(20)

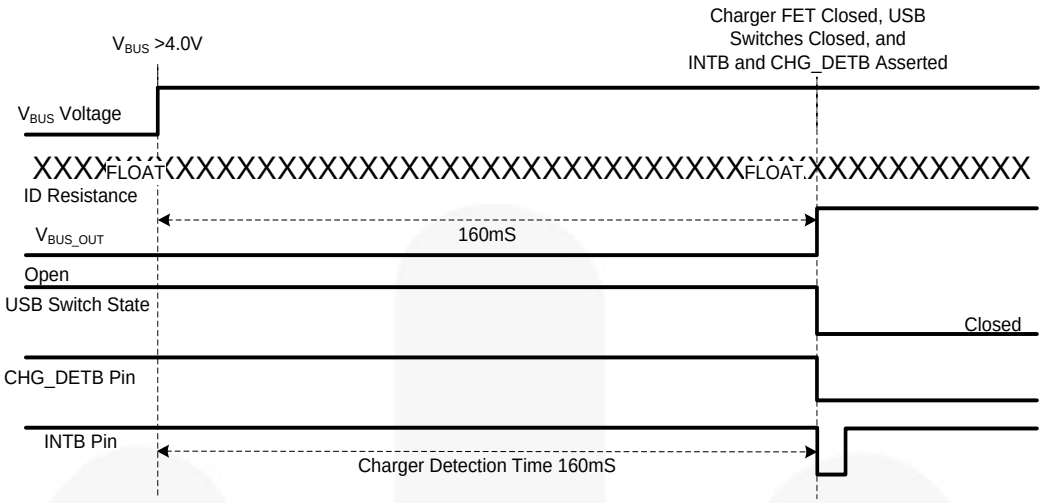


Figure 10. USB Dedicated Charging Port (DCP) or Charging Downstream Port (CDP) Attach Timing[20]

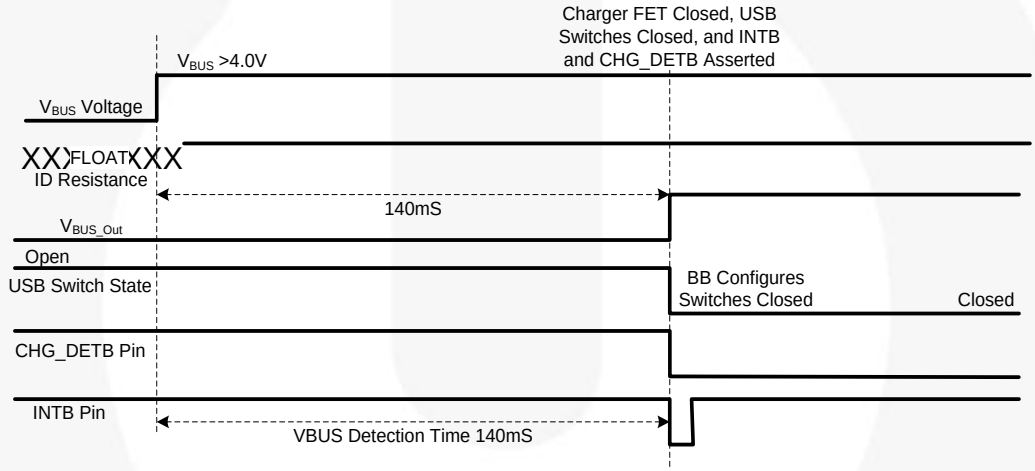


Figure 11. Car Kit Type-1 and Type-2 Attach Timing

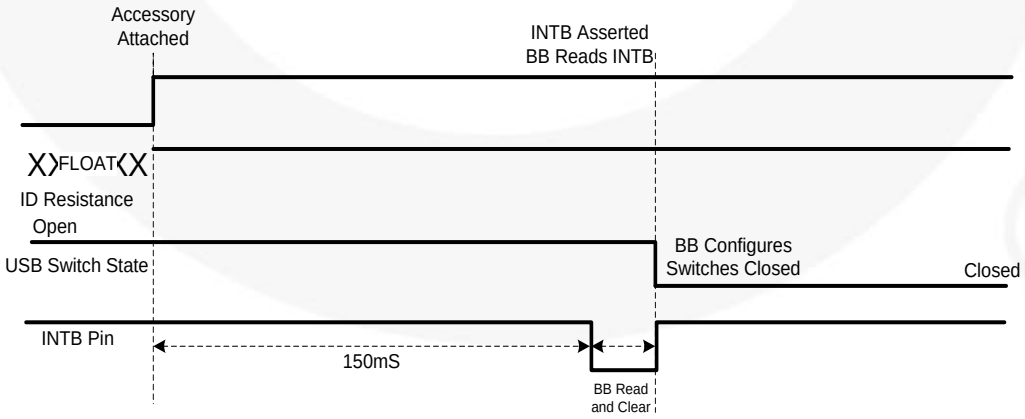


Figure 12. ID-Based Accessories, No V_{BUS_IN} Attach Timing[21]

Notes:

20. USB Switch State timing is based on Automatic Switching mode (EN_MAN_SW = 0). Automatic switching excludes DCP.
21. ID_CON resistance detection based on default Timing Set and Applications register values and on initial ID_CON accessory attach only (50 ms Resistor Detection Time with three ID checks on initial attach = 150 ms typical detection time).

19. Bit Definitions

Table 6. I^2C Register Map

Address	Register	Type	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01H	Device ID	R	00010000	Version ID					Do Not Use		
02H	Control	R/W	11010001	DCD Timeout EN	RESETB	ID_DIS	EN_MAN_SW	Do Not Use	Do Not Use	Do Not Use	INT Mask
03H	Interrupt	R/C	00000000	Do Not Use	OCP Change	OVP Change	MIC_OVP Change	Resistor Code Change	V_{BUS}_Valid Change	BC1.2_Complete	Do Not Use
05H	Interrupt Mask	R/W	00000000	Do Not Use	OCP	OVP	MIC_OVP	Resistor Code Change	V_{BUS}_Valid	BC1.2_Complete	Do Not Use
07H	Resistor Code	R	00000000	Do Not Use	Do Not Use	Do Not Use	Resistor Code				
08H	Timing Set	R/W	00000000	Do Not Use				Resistor Detection Time			
09H	Status	R	00000000	ID_SHORT	OCP	OVP	MIC_OVP	/ID_FLOAT	V_{BUS}_Valid	BC1.2_Active	DCD
0AH	Device Type	R	00000000	Do Not Use	Do Not Use	Dock	Do Not Use	Do Not Use	USB Dedicated Charging Port (DCP)	USB Charging Downstream Port (CDP)	USB Standard Downstream Port (SDP)
0BH	DAC SAR	R	00000000	DAC SAR Value							
13H	Manual SW	R/W	00100111	D- Switching			D+ Switching			V_{BUS} Switching	
14H	Manual CHG_CTRL	R/W	00000000	Do Not Use	Do Not Use	Do Not Use	Assert CHG_DETB	MIC_OVP_EN	Assert_D+	Do Not Use	
1BH	Applications1	R/W	X0001000	Do Not Use	Do Not Use	Do Not Use	# of Consecutive ID Matches for Attach			Do Not Use	Do Not Use
1CH	Applications2	R/W	XXXX0101	Do Not Use	Do Not Use	Do Not Use	Do Not Use	# ID Checks for Resistor Code Change		Max. Capacitance on ID	

Table 7. Device ID

- Address: 01H
- Reset Value: 00010000
- Type: Read

Bit #	Name	Size (Bits)	Description
7:3	Version ID	5	Rev 0.0=00010
2:0	Do Not Use	3	Do not use

Table 8. Control

- Address: 02H
- Reset Value: 11010001
- Type: Read/Write

Bit #	Name	Size (Bits)	Description
7	DCDTimeout_EN	1	1: DCD timeout is enabled. 0: DCD timeout is disabled.
6	RESETB	1	1: Do nothing. 0: Reset FSA9285A – resets all of FSA9285A except the Control register (02H), Manual SW (13H), and Manual CHG_CTRL(14H). **Note**: This bit is momentarily set to 0 on a write. It immediately reverts to 1.
5	ID_DIS	1	1: ID_CON resistor detection is disabled after a resistance is detected on ID_CON. 0: ID_CON resistor detection is enabled after a resistance is detected on ID_CON. **Note**: The FSA9285A continues to monitor for an ID_FLOAT condition.
4	EN_MAN_SW	1	1: Configure switches based on Manual SW register settings.

Bit #	Name	Size (Bits)	Description
			0: Use only defined automatic switch settings. This bit needs to be cleared in case of a weak battery explicitly or the device must be defaulted via a V_{DDIO} reset for the dead battery case to operate properly.
3	Do Not Use	1	Do not use.
2	Do Not Use	1	Do not use.
1	Do Not Use	1	Do not use.
0	INT Mask	1	1: Mask Interrupt – Do not interrupt baseband processor when a bit is set in the Interrupt register. 0: Unmask Interrupt – Interrupt baseband processor if any bit is set in the Interrupt register.

Table 9. Interrupt

- Address: 03H
- Reset Value: 00000000
- Type: Read/Clear

Bit #	Name	Size (Bits)	Description
7	Do Not Use	1	N/A
6	OCP Change	1	1: OCP state changed. 0: OCP state has not changed.
5	OVP Change	1	1: OVP state changed. 0: OVP state has not changed.
4	MIC_OVP Change	1	1: MIC OVP state changed. 0: MIC OVP state not changed.
3	Resistor Code Change	1	1: Resistor Code value changed. 0: Resistor Code value has not changed. **Note**: This interrupt is disabled when ID_DIS=1. The FSA9285A interrupts if transitioning from a non-zero Resistor Code to a Resistor Code=zero (ID_CON floating).
2	V_{BUS}_Valid Change	1	1: V_{BUS}_Valid state changed. 0: V_{BUS}_Valid state has not changed.
1	BC1.2_Complete	1	1: BC1.2 charger detection complete. 0: No change in BC1.2 charger detection status.
0	Do Not Use	1	N/A

Table 10. Interrupt Mask

- Address: 05H
- Reset Value: 00000000
- Type: Read/Write

Bit #	Name	Size (Bits)	Description
7	Do Not Use	1	N/A
6	OCP	1	1: Mask OCP state-change interrupt. 0: Do not mask OCP state-change interrupt.
5	OVP	1	1: Mask OVP state-change interrupt. 0: Do not mask OVP state-change interrupt.
4	MIC_OVP	1	1: Mask MIC_OVP state-change interrupt. 0: Do not mask MIC_OVP state-change interrupt.

Bit #	Name	Size (Bits)	Description
3	Resistor Code Change	1	1: Mask Resistor Code value-change interrupt. 0: Do not mask Resistor Code value-change interrupt.
2	V_{BUS}_Valid	1	1: Mask V_{BUS_Valid} state-change interrupt. 0: Do not mask V_{BUS_Valid} state-change interrupt.
1	BC1.2_Complete	1	1: Mask BC1.2_complete interrupt. 0: Do not mask BC1.2_complete interrupt.
0	Do Not Use	1	N/A

Table 11. Resistor Code

- Address: 07H
- Reset Value: 00000000
- Type: Read

Bit #	Name	Size (Bits)	Description
7:5	Do Not Use	3	N/A
4:0	Resistor Code	5	Resistor code value read from ID_CON *(see Table 3 Resistor Identification).*

Table 12. Timing Set

- Address: 08H
- Reset Value: 00000000
- Type: Read/Write

Bit #	Name	Size (Bits)	Description
7:4	Do Not Use	4	N/A
3:0	Resistor Detection Time	4	Time to complete the ID_CON resistance measurement for accessory detection *(see Table 13).*

Table 13. Timing Table for Timing Set Register

Setting Value	Resistor Detection Time (ms)
0000	50
0001	100
0010	150
0011	200
0100	300
0101	400
0110	500
0111	600
1000	700
1001	800
1010	900
1011	1000
1100	
1101-1111	

Table 14. Status

- Address: 09H
- Reset Value: 00000000
- Type: Read/Write

Bit #	Name	Size (Bits)	Description
7	ID_SHORT	1	1: ID_SHORT detected. 0: ID_SHORT not detected.
6	OCP	1	1: V_{BUS} in over-current state. 0: V_{BUS} not in over-current state.
5	OVP	1	1: V_{BUS} in over-voltage state. 0: V_{BUS} not in over-voltage state.
4	MIC_OVP	1	1: MIC in over-voltage state 0: MIC not in over-voltage state
3	/ID_FLOAT	1	1: ID_CON not floating (resistor detected). 0: ID_CON floating (no resistor detected).
2	V_{BUS}_Valid	1	1: V_{BUS} is valid. 0: V_{BUS} is not valid.
1	BC1.2_Active	1	1: BC1.2 is active. (This is true if a connect is attempted with DCD Timeout disabled and no DCD.) 0: BC1.2 IDLE.
0	DCD	1	1: Data contact detected on last charger-detect sequence. 0: No data contact detected on last charger-detect sequence.

Table 15. Device Type

- Address: 0AH
- Reset Value: 00000000
- Type: Read

Bit #	Name	Size (Bits)	Description
7	Do Not Use	1	Do not use.
6	Do Not Use	1	Do not use.
5	Dock	1	1: Charging dock detected. 0: Charging dock not detected.
4	Do Not Use	1	Do not use.
3	Do Not Use	1	Do not use.
2	DCP	1	1: USB dedicated charging port (DCP) charger detected. 0: USB dedicated charging port (DCP) charger not detected.
1	CDP	1	1: USB charging downstream port (CDP) charger detected. 0: USB charging downstream port (CDP) charger not detected.
0	SDP	1	1: USB standard downstream port (SDP) detected. 0: USB standard downstream port (SDP) not detected.

Table 16. DAC SAR

- Address: 0BH
- Reset Value: 00000000
- Type: Read

Bit #	Name	Size (Bits)	Description
7:0	DAC_SAR	8	DAC_SAR Value – Indicates raw 8-bit resistance value detected *(see Table 3 Resistor Identification).*

Table 17. Manual SW[22]

- Address: 13H
- Reset Value: 00100111
- Type: Read/Write

Bit #	Name	Size (Bits)	Description
7:5	DM_CON Switching	3	000: Open all switches. 001: DM_CON connected to DM_HOST1 of USB port. 010: DM_CON connected to Audio_L. 011: DM_CON connected to DM_HOST2 of USB port.
4:2	DP_CON Switching	3	000: Open all switches. 001: DP_CON connected to DP_HOST1 of USB port. 010: DP_CON connected to Audio_R. 011: DP_CON connected to DP_HOST2 of USB port. 100: DP_CON connected to MIC.
1:0	V_{BUS_IN} Switching	2	00: Open all switches. 01: Do not use. 10: V_{BUS_IN} connected to MIC. 11: V_{BUS_IN} connected to V_{BUS_OUT} (phone sinks current from attached accessory).[23]

Notes:

22. When changing manual switch configurations on a single attach, the accessory must pass through an “Open All Switches” state between configurations. Manual Modes require the EN_MAN_SW Manual Mode bit in the Control register (02H) to be set.
23. V_{BUS_IN} must be valid for the charger FET to close in manual FET switching.

Table 18. Manual CHG_CTRL

- Address: 14H
- Reset Value: 00000000
- Type: Read/Write

Bit #	Name	Size (Bits)	Description
7:5	Do Not Use	3	N/A
4	Assert CHG_DETB	1	1: Assert CHG_DETB LOW. 0: Normal operation (CHG_DETB asserted LOW for DCP, CDP, ACA, and Car Kit Type 1/2; CHG_DETB is HIGH otherwise.) **Note**: EN_MAN_SW is not required for this bit to take effect.
3	MIC_OVP_EN	1	1: Enable MIC_OVP (only use when MIC is connected to V_{BUS}). 0: Do not enable MIC_OVP. **Note**: EN_MAN_SW is not required for this bit to take effect.
2	Assert_D+	1	1: Force 0.6 V on DP_CON. 0: Do not force 0.6 V on DP_CON. **Note**: EN_MAN_SW is not required for this bit to take effect, V_{BUS} must be valid.
1:0	Do Not Use	2	N/A

Table 19. Applications1

- Address: 1BH
- Reset Value: X0001000
- Type: Read/Write

Bit #	Name	Size (Bits)	Description
7:5	Do Not Use	3	N/A
4:2	# Consecutive ID Matches for Attach	3	000: 1 001: 2 010: 3 011: 4 100: 5 101: 6 110: 7 111: 8
1:0	Do Not Use	2	N/A

Table 20. Applications2

- Address: 1CH
- Reset Value: XXXX0101
- Type: Read/Write

Bit #	Name	Size (Bits)	Description
7:4	Do Not Use	4	N/A
3:2	# ID Checks for Resistor Code Change	2	00: 1 01: 2 10: 3 11: 4
1:0	Max. Capacitance on ID	2	00: 500 pF 01: 1 nF 10: 1.5 nF 11: 2 nF

20. Reference Schematic

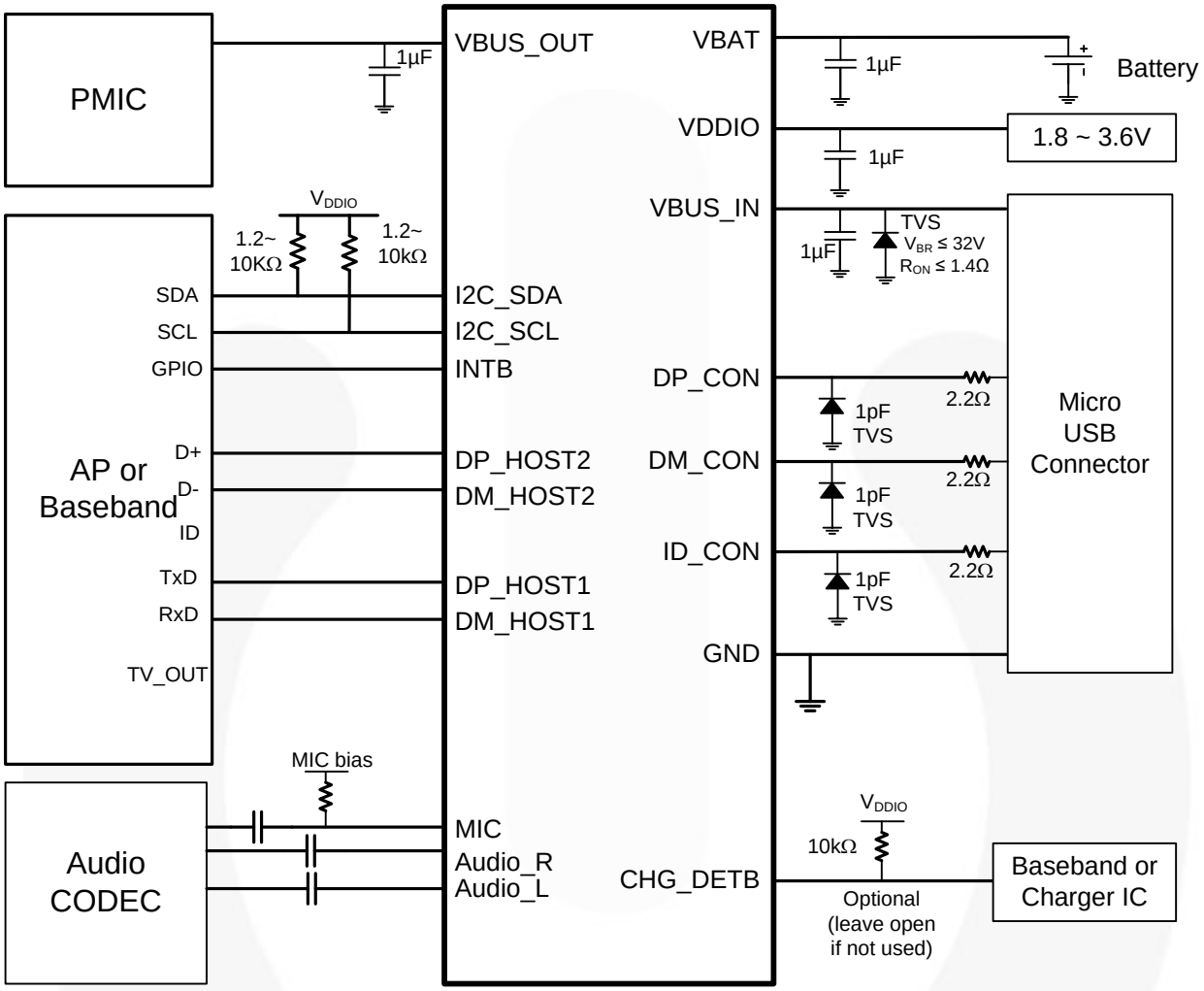


Figure 13. Reference Schematic

21. Layout Guidelines

PCB Layout Guidelines for High-Speed USB Signal Integrity

1. Place the FSA9285A as close to the USB controller as possible. Shorter traces mean less loss, less chance of picking up stray noise, and less radiated EMI.
   a) Keep the distance between the USB controller and the device less than 25.4 mm (or one inch <1 in).
   b) For best results, keep this distance <18 mm. This keeps it less than one quarter (¼) of the transmission electrical length.
2. Use an impedance calculator to ensure 90 Ω differential impedance for DP_COM/DM_CON lines.
3. Select the best transmission line for the application.
   a) For example, for a densely populated board, select an edge-coupled differential stripline.
4. Minimize the use of vias and keep HS USB lines on same plane in the stack.
   a) Vias are an interruption in the impedance of the transmission line and should be avoided.
   b) Try to avoid routing schemes that generally force the use of at least two vias: one on each end to get the signal to and from the surface.
5. Cross lines, only if necessary, orthogonally to avoid noise coupling (traces running in parallel couple).
6. If possible, separate HS USB lines with GND to improve isolation.
   a) Avoid routing GND, power, or components close to the transmission lines to avoid impedance discontinuities.
7. Match transmission line pairs as much as possible to improve skew performance.
8. Avoid sharp bends in PCB traces; a chamfer or rounding is generally preferred.
9. Place decoupling for power pins as close to the device as possible.
   a) Use low-ESR capacitors for decoupling if possible.
   b) If needed, a tuned PI filter should be used to negate the effects of switching power supplies and other noise sources.

Layout for Global System for Mobile Communication (GSM) Time Division Multiple Channel (TDMA) Buzz Reduction

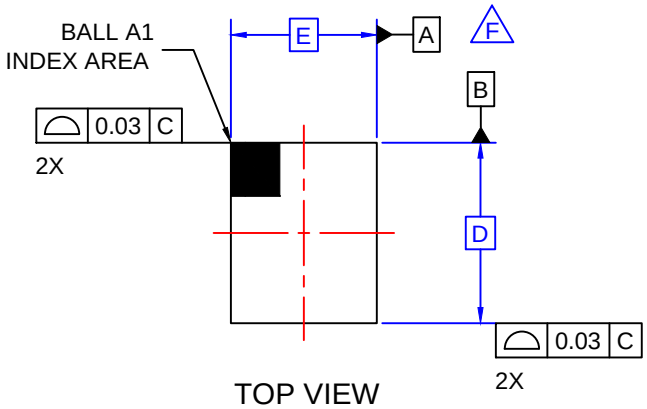
There are two possible mechanisms for TDMA/GSM noise to negatively impact FSA9285A device's performance. The first is the result of large current draw by the phone transmitter during active signaling when the transmitter is at full or almost full power. With the phone transmitter dumping large amounts of current in the phone GND plane; it is possible for there to be temporary voltage excursions in the GND plane if not properly designed. This noise can be coupled back up through the GND plane into the FSA9285A device and, although the FSA9285A has very good isolation; if the GND noise amplitude is large enough, it can result in noise coupling to the VBUS_In / MIC pin. The second path for GSM noise is through electromagnetic coupling onto the signal lines themselves.

Ordering Information

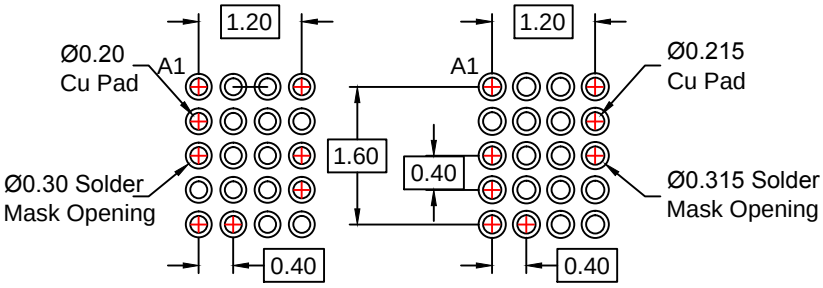
Part Number	Operating Temperature Range	Top Mark	Package
FSA9285AUCX	-40 to +85°C	NQ	20-Lead, WLCSP (2.010 x 1.672 x 0.625 mm, 0.4 mm Pitch)

Product-Specific Package Dimensions

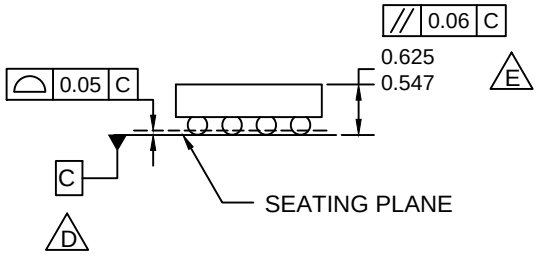
Product	D	E	X	Y
FSA9285AUCX	2.010 mm	1.672 mm	0.236 mm	0.205 mm

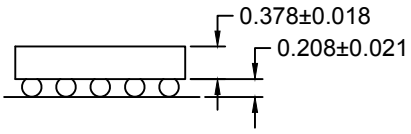


TOP VIEW

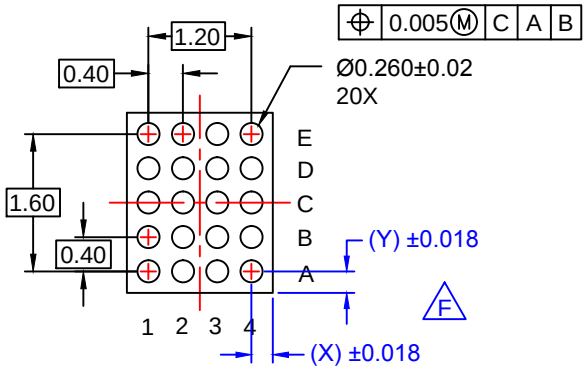


RECOMMENDED LAND PATTERN
(NSMD TYPE)





SIDE VIEWS



BOTTOM VIEW

NOTES:

A. NO JEDEC REGISTRATION APPLIES.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCE PER ASMEY14.5M, 2009.
D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
E. PACKAGE NOMINAL HEIGHT IS 586 MICRONS ±39 MICRONS (547-625 MICRONS).
F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.
G. DRAWING FILNAME: MKT-UC020AArev4.

FAIRCHILD

PUBLICATION ORDERING INFORMATION

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