Title	***Reference Design Report for a 36 W Continuous, 72 W Peak Power Supply Using PKS606YN***
Specification	90 – 265 VAC Input, 12 V, 36 W Continuous (72 W Peak) Output
Application	Variable Speed Motor Drive
Author	Power Integrations Applications Department
Document Number	RDR-128
Date	August 16, 2007
Revision	1.0

Summary and Features

- Replaces a two-stage linear power supply and chopper circuit with a simple single-stage design
- Eliminates the chopper circuits normally used to achieve variable-speed control of DC motors
- Motor speed is controllable by a small potentiometer or a 3.6 V to 10 V variable DC voltage
- Easily meets CISPR-22 / EN55022B limits with E-Shields and Frequency jittering feature.

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This document is an engineering report describing a motor drive power supply capable of delivering up to 36 W of continuous power and up to 72 W of peak power, utilizing a PKS606YN device. This power supply is intended as a demonstration platform for the *PeakSwitch* family of devices and their application in motor drives. The *PeakSwitch* family of devices is ideally suited to this role due to their ability to provide very high peak power for short periods of time, as is often encountered in motor drive applications.

This document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit board layout and performance data.

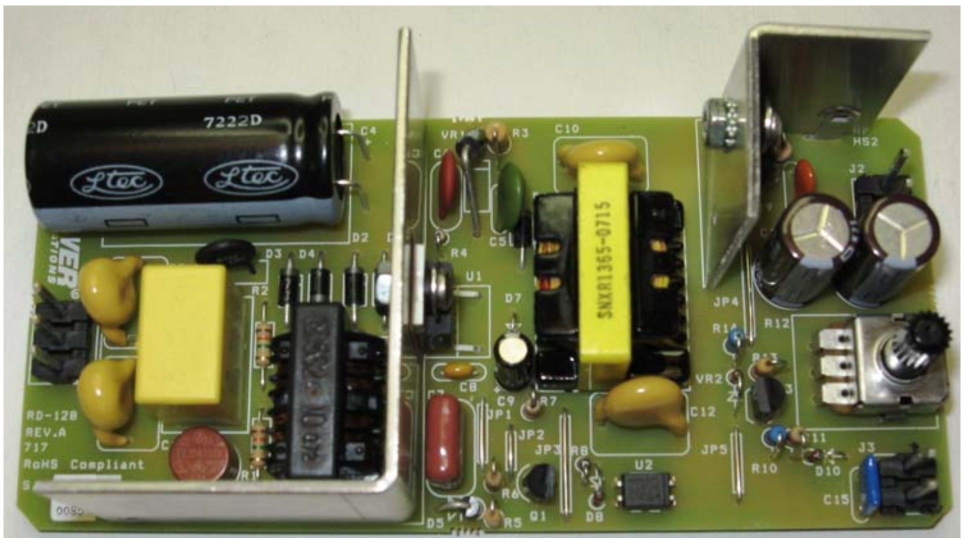

Figure 1 – Populated Circuit Board Photograph.

2 Power Supply Specification

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power (230 VAC)				0.3	W	
Output						
Output Voltage 1	V_{OUT1}	11.5	12	12.5	V	± 5%
Output Ripple Voltage 1	$V_{RIPPLE1}$		800		mV	20 MHz bandwidth
Continuous Output Current 1	I_{OUT1}		3		A	
Peak Output Current 1	I_{OUTPK}		6.0		A	
Total Output Power						
Continuous Output Power	P_{OUT}		36		W	
Peak Output Power	P_{OUT_PEAK}		72		W	
Efficiency						
Full Load	η	80			%	Measured at P_{OUT} 25 ^{o}C
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Safety		Designed to meet IEC950, UL1950 Class II				
Surge		2			kV	1.2/50 μs surge, IEC 1000-4-5, Series Impedance: Differential Mode: 2 Ω Common Mode: 12 Ω
Ambient Temperature	T_{AMB}	0		40	^{o}C	Free convection, sea level

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3 Schematic

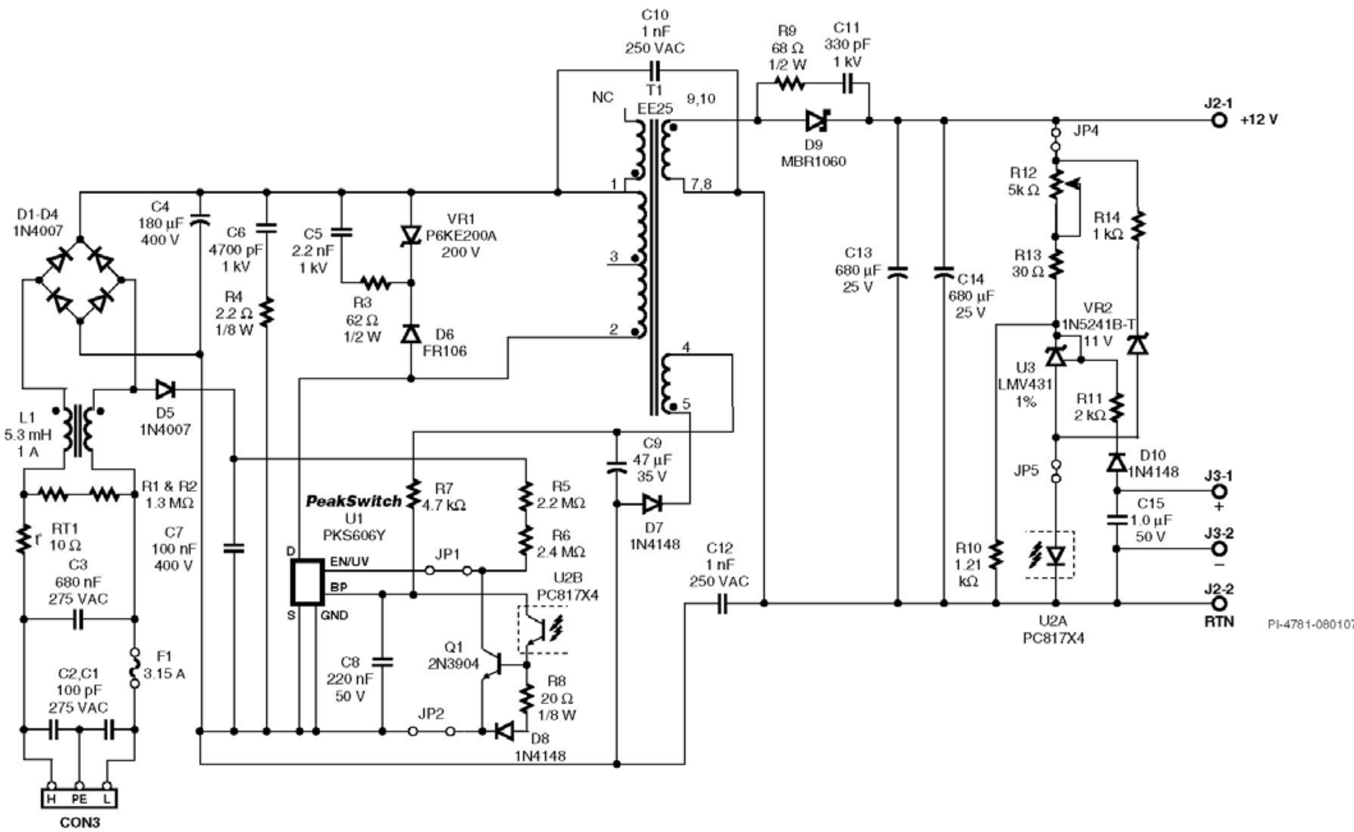

Figure 2 – Schematic.

4 Circuit Description

The motor drive power supply shown in Figure 1 is a switch mode power supply design utilizing the flyback topology.

4.1 Input EMI Filtering

Differential mode EMI filtering is provided by X-capacitor C3. Y-capacitors C1, C2, C10 and C12, together with the common-mode choke L1, provide common-mode EMI filtering. Additionally the transformer *E-Shields*™, together with the frequency jittering features, provide adequate EMI margins.

4.2 PeakSwitch Primary

Fuse F1 protects the power supply from a catastrophic failure due to a short circuit fault. A high voltage DC bus is created from the AC line voltage by the full-wave rectifier formed by diodes D1-D4. Capacitor C4 smoothes and filters the rectified AC voltage.

The PKS606YN (U1) integrates a high voltage MOSFET, along with startup and all necessary control circuitry.

During the MOSFET's on-time, current flows through the primary of transformer T1, storing energy in the transformer core.

During the turn off event, the voltage across the primary winding reverses. A voltage equal to the sum of DC bus voltage and the reflected output voltage (VOR) appears across the DRAIN and SOURCE of the PeakSwitch, with an additional spike generated by the leakage inductance. A primary clamp circuit formed by D6, VR1, R3 and C5 limits this voltage and resets the leakage energy prior to the next switching cycle.

Diode D7 rectifies the supply's bias winding while capacitor C9 provides DC filtering. This bias supply is connected to the *PeakSwitch*'s BP pin via R7, which powers the device during normal operation.

4.3 Under-voltage Protection and Fast AC Reset circuit

Under-voltage shutdown is implemented by a separate line rectifying diode, D5, which charges capacitor C7. Resistors R5 and R6 program the UV start-up voltage to approximately 104 VDC, which is the DC voltage across C7, at which a current equal to 25 µA flows into the EN/UV pin.

This separate AC line sense network (formed by D5, C7) allows the *PeakSwitch* to identify the cause of a fault condition. If the input voltage is above the under-voltage threshold and the EN/UV pin has not been pulled low for 30 ms, a fault condition is assumed, and the *PeakSwitch* latches off. Once the supply is latched off, the AC line voltage must be removed to allow capacitor C7 to discharge and allow the current into the EN/UV pin to fall below 25 µA.

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If the EN/UV pin has not been pulled low for 30 ms and the input voltage is below the under-voltage threshold, then the loss of regulation is assumed to be due to a low line condition, and the *PeakSwitch* will stop switching until the under-voltage threshold is exceeded again.

4.4 Output Rectification and Filtering

Diode D9 rectifies the output voltage while capacitors C13 and C14 provide output filtering. The output capacitor current ripple rating is chosen to be sufficient for the maximum rated *continuous/average* load. Resistor R9 and capacitor C11 form a snubber network across diode D9, which reduces high frequency ringing that occurs during the diode turn off event.

4.5 Output Feedback

The *PeakSwitch* family of devices uses a simple on/off control scheme. When a current greater than 240 µA is drawn from the EN/UV pin of U1, the subsequent switching cycle is disabled. The EN/UV pin is pulled low whenever phototransistor U2B of the optocoupler conducts enough current through R8, thus forward biasing D8 and turning on transistor Q1. Transistor Q1 then pulls current out of the EN/UV pin. Having the phototransistor's collector connected to the bypass pin of the *PeakSwitch* gives a collector to emitter voltage (V_{CE}) of approximately 5.8 V, which allows the phototransistor to source current more effectively while using the high gain, small signal transistor Q1 to draw the current from the EN/UV pin. Optocoupler U2's high CTR (300% – 600%) ensures a fast control loop response. Diode D8 is placed close to Q1 and thus provides thermal compensation against Q1's V_{BE} drop.

The output voltage is variable to allow for speed control of the DC motor. An adjustable shunt regulator, U3, has its cathode tied to its reference, making it behave as a voltage reference at approximately 1.24 V above the 1.1 V optocoupler's LED (U2A) drop.

When no external control voltage is applied at terminals J3, diode D10 remains reverse biased and potentiometer R12 controls the voltage of the divider network formed by itself, R13 and R10. Decreasing the value of R12 programs a new voltage set-point (and also a new speed), and the feedback loop now regulates to a lower output voltage. Setting potentiometer R12 to its minimum value regulates the output down to 2.35 V. An 11 V zener diode (VR2) is in place to ensure the output voltage does not regulate too far above 12 V, as may occur due to the large tolerances of most potentiometers (which may be as high as ±20%).

The supply's output voltage may also be controlled by an external DC control voltage applied at J3, with amplitude between 0 V and 10 V. Applying an external voltage above 3.5 V at J3 will forward bias diode D10 and will set the reference and cathode pin of the shunt regulator to the external control voltage. Applying a higher external control voltage allows more current to flow through the LED of the optocoupler and thus reduces the supply's output voltage. If 10 V is applied at J3, the supply shuts down completely. Reducing the external control voltage after a shut down will start the power supply again.

5 PCB Layout

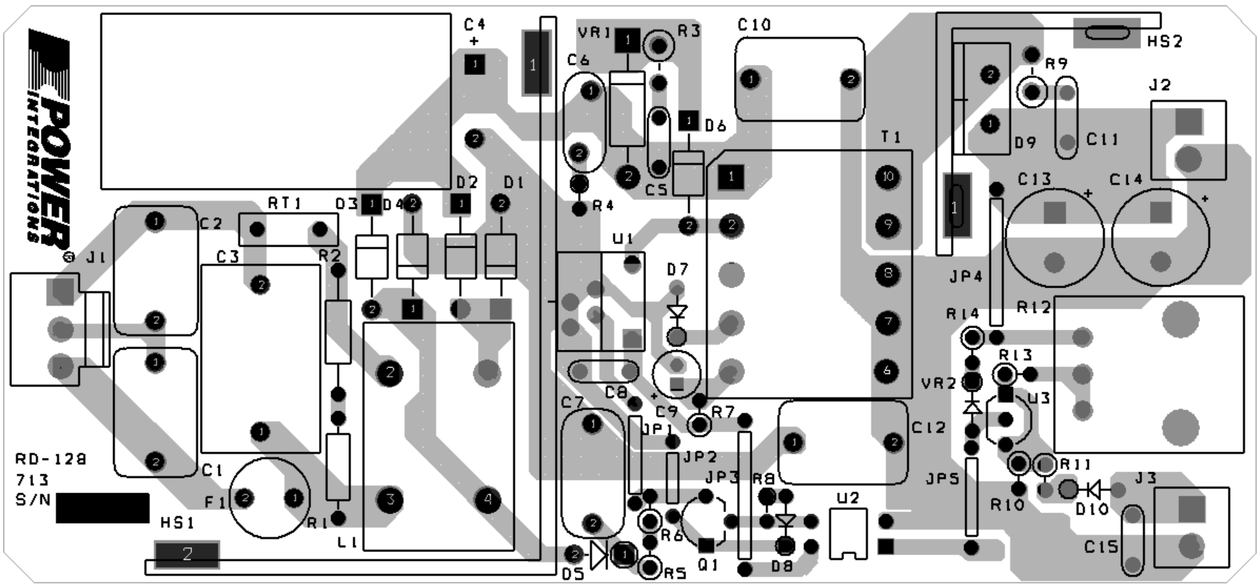

Figure 3 – Printed Circuit Layout.

6 Bill of Materials

Item	Qty	Ref	Description	Mfg	Mfg Part Number
1	2	C1 C2	100 pF, Ceramic, Y1	Panasonic	ECK-ANA101MB
2	1	C3	680 nF, 275 VAC, Film,MPX Series, X2	Carli	PX684K3ID6
3	1	C4	180 uF, 400 V, Electrolytic, Low ESR, (18 x 40)	Nippon Chemi-Con	EPAG401ELL181MM40S
4	1	C5	2.2 nF, 1 kV, Disc Ceramic	NIC Components Corp	NCD222K1KVY5FF
5	1	C6	4700pF, 1 kV, Thru Hole, Disc Ceramic	Vishay/Sprague	562R5GAD47
6	1	C7	100 nF, 400 V, Film	Panasonic	ECQ-E4104KF
7	1	C8	220 nF, 50 V, Ceramic, Z5U, 0.2" L.S.	Kemet	C322C224M5U5CA
8	1	C9	47 uF, 35 V, Electrolytic, Gen. Purpose, (5 x 11)	Panasonic	ECA-1VHG470
9	2	C10 C12	1 nF, Ceramic, Y1	Panasonic	ECK-ANA102MB
10	1	C11	330 pF, 1 kV, Disc Ceramic	Vishay	562R5GAT33
11	2	C13 C14	680 uF, 25 V, Electrolytic, Very Low ESR, 23 mOhm, (10 x 20)	Nippon Chemi-Con	EKZE250ELL681MJ20S
12	1	C15	1.0 uF, 50 V, Ceramic, X7R	Epcos	B37984M5105K000
13	5	D1 D2 D3 D4 D5	1000 V, 1 A, Rectifier, DO-41	Vishay	1N4007
14	1	D6	800 V, 1 A, Fast Recovery Diode, 500 ns, DO-41	Diodes Inc.	FR106
15	3	D7 D8 D10	75 V, 300 mA, Fast Switching, DO-35	Vishay	1N4148
16	1	D9	60 V, 10 A, Schottky, TO-220AC	Vishay	MBR1060
17	1	F1	3.15 A, 250V, Slow, TR5	Wickman	3721315041
18	1	HS PAD1	HEATSINK PAD, TO-220, Sil-Pad 1000	Bergpuist	1009-58
19	1	HS1	HEATSINK/Alum, TO220 1 hole, 2 mtg pins	Clark Precision Sheetmetal	60-00012-00
20	1	HS2	HEATSINK/Alum, TO220 1 hole, 2 mtg pins	Clark Precision Sheetmetal	60-00020-00
21	1	J1	3 Position (1 x 3) header, 0.156 pitch, Vertical	Molex	26-48-1031
22	2	J2 J3	2 Position (1 x 2) header, 0.156 pitch, Vertical	Molex	26-48-1021
23	2	JP1 JP5	Wire Jumper, Non insulated, 22 AWG, 0.4 in	Alpha	298
24	1	JP2	Wire Jumper, Non insulated, 22 AWG, 0.3 in	Alpha	298
25	2	JP3 JP4	Wire Jumper, Non insulated, 22 AWG, 0.6 in	Alpha	298

26	1	L1	5.3 mH, 1 A, Common Mode Choke	Panasonic	ELF15N010A
27	2	NUT1 NUT2	Nut, Hex, Kep 4-40, S ZN Cr3 plateing RoHS		
28	1	Q1	NPN, Small Signal BJT, 40 V, 0.2 A, TO-92	On Semiconductor	2N3904RLRAG
29	2	R1 R2	1.3 M, 5%, 1/4 W, Carbon Film	Yageo	CFR-25JB-1M3
30	1	R3	62 R, 5%, 1/2 W, Carbon Film	Yageo	CFR-50JB-62R
31	1	R4	2.2 R, 5%, 1/8 W, Carbon Film	Yageo	CFR-12JB-2R2
32	1	R5	2.2 M, 5%, 1/4 W, Carbon Film	Yageo	CFR-25JB-2M2
33	1	R6	2.4 M, 5%, 1/4 W, Carbon Film	Yageo	CFR-25JB-2M4
34	1	R7	4.7 k, 5%, 1/4 W, Carbon Film	Yageo	CFR-25JB-4K7
35	1	R8	20 R, 5%, 1/8 W, Carbon Film	Yageo	CFR-12JB-20R
36	1	R9	68 R, 5%, 1/2 W, Carbon Film	Yageo	CFR-50JB-68R
37	1	R10	1.21 k, 1%, 1/4 W, Metal Film	Yageo	MFR-25FBF-1K21
38	1	R11	2 k, 5%, 1/4 W, Carbon Film	Yageo	CFR-25JB-2K0
39	1	R12	5 k,Pot, 20%, 1/8 W, Vertical	CTS Corp.	296UD502B1N
40	1	R13	30 R, 5%, 1/4 W, Carbon Film	Yageo	CFR-25JB-30R
41	1	R14	1 k, 1%, 1/4 W, Metal Film	Yageo	MFR-25FBF-1K00
42	1	RT1	NTC Thermistor, 0.34 Ohms, 1.7 A	Thermometrics	CL-120
43	2	SCREW1 SCREW2	SCREW MACHINE PHIL 4-40X5/16 SS	Building Fasteners	PMSSS 440 0031 PH
44	1	T1	Transformer, 10 Pins, Vertical	Yih-Hwa Enterprises Santronics	YW-360-02B SNX R1365
45	1	U1	PeakSwitch, PKS606YN, TO-220-7C	Power Integrations	PKS606YN
46	1	U2	Opto coupler, 35 V, CTR 300-600%, 4-DIP	Sharp	PC817XJ0000F
47	1	U3	1.24V Shunt Reg IC	National Semiconductor	LMV431ACZ
48	1	VR1	200 V, 600 W, 5%, TVS, DO204AC (DO-15)	OnSemi	P6KE200ARLG
49	1	VR2	11 V, 500 mW, 5%, DO-35	Diodes Inc	1N5241B-T
50	2	WASHER1 WASHER2	WASHER FLAT #4 SS	Building Fasteners	FWSS 004
51	1	WASHER3	Washer Nylon Shoulder #4	Keystone	3049

Note – Parts listed above are all RoHS compliant

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7 Transformer Specification

7.1 Electrical Diagram

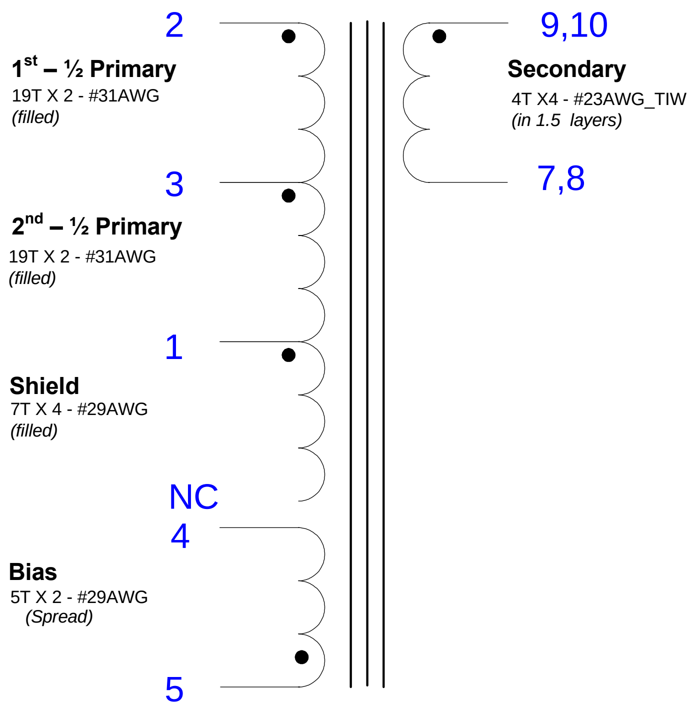

Figure 4 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from Pins 1-5 to Pins 7 and 10	3000 VAC
Primary Inductance	Pins 1-2, all other windings open, measured at 100 kHz, 0.4 VRMS	148 μH, ± 12%
Resonant Frequency	Pins 1-2, all other windings open	3 MHz (Min) 4 MHz (Max)
Primary Leakage Inductance	Pins 3-4, with Pins 8-9 shorted, measured at 100 kHz, 0.4 VRMS	6 μH (Max.)

7.3 Materials

Item	Description
[1]	Core: PC40EE25-Z, TDK or equivalent gapped for AL of 104 nH/T^2. Gap approx. 0.47 mm.
[2]	Bobbin: EE25 Vertical 10 pin
[3]	Magnet Wire: #31 AWG
[4]	Magnet Wire: #29 AWG
[5]	Triple Insulated Wire: #23 AWG
[6]	Tape, 3M 1298 Polyester Film, 2.0 mil thick, 10.7 mm wide
[7]	Varnish

7.4 Transformer Build Diagram

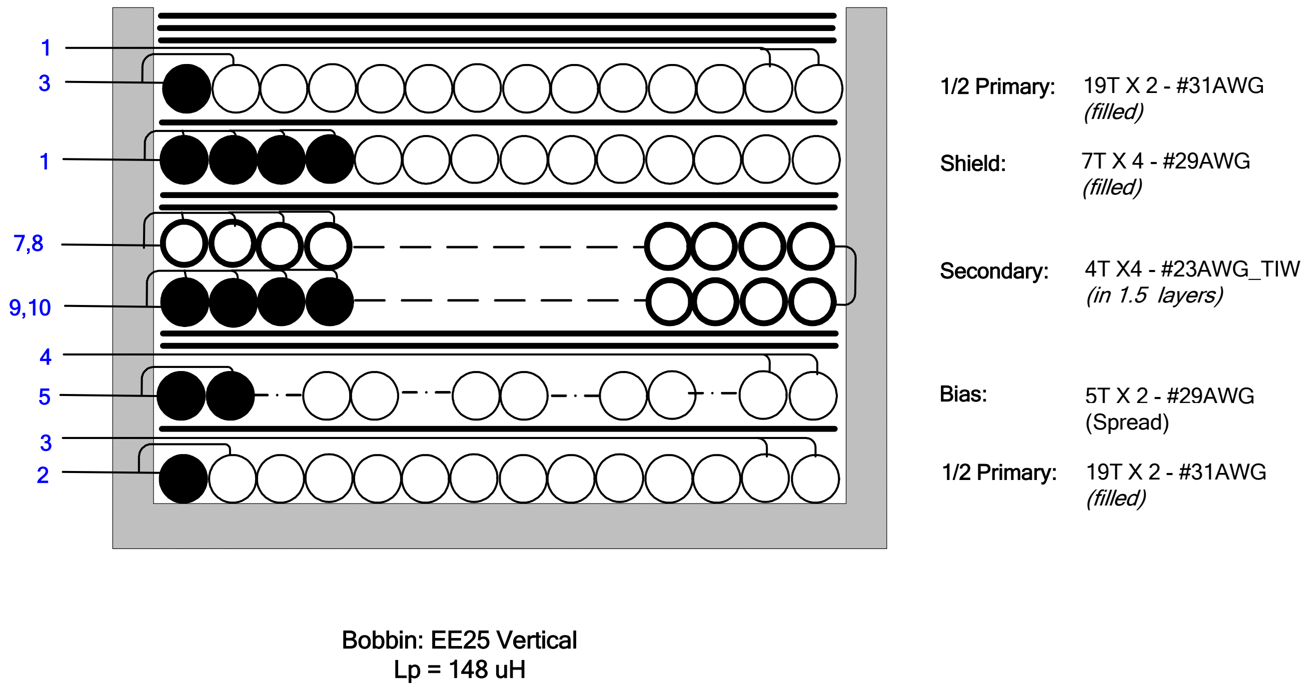

Figure 5 – Transformer Build Diagram.

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7.5 Transformer Construction

Bobbin Preparation	Pin side of the bobbin is oriented to the left hand side. Winding direction is clockwise when viewed from the non-pin side.
1st Half Primary Winding	Start on pin 2, wind 19 bi-filar turns of item [3], Magnet Wire: #31 AWG, from left to right with tight tension and bring the wire back across the bobbin and terminate the winding on pin 3.
Insulation	Apply 1 layer of item [6], 3M 1298 Polyester Film tape, for insulation.
Bias Winding	Start on pin 5, wind 5 bi-filar turns of item [4], Magnet Wire: #29 AWG, from left to right, spreading the windings evenly across the bobbin. Bring the wire back across the bobbin and terminate the winding on pin 4.
Insulation	Apply 2 layers of item [6], 3M 1298 Polyester Film tape, for insulation.
Secondary Winding	Start on pin 9 and 10 using 2 wires for each pin. Wind 4 quad-filar turns of item [5], #23 AWG Triple Insulated Wire, from right to left. Continue winding the second layer from right to left, spreading the turns evenly across the bobbin. Terminate the winding on pins 7 and 8 using two wires for each pin.
Insulation	Apply 2 layers of item [6], 3M 1298 Polyester Film tape, for insulation.
Shield Winding	Start on pin 1 and wind 7 quad-filar turns of item [4], Magnet Wire: #29 AWG from left to right with tight tension across the bobbin. Cut and finish the end.
2nd Half Primary Winding	Start on pin 3, wind 19 bi-filar turns of item [3], Magnet Wire: #31 AWG, from left to right with tight tension and bring the wire back across the bobbin and terminate the winding on pin 1.
Insulation	Apply 3 layers of item [6], 3M 1298 Polyester Film tape, for insulation
Core Assembly	Assemble and secure core halves.
Varnish	Dip varnish assembled transformer with item [7], varnish.

8 Transformer Spreadsheet

ACDC_PeakSwitch_020107; Rev.1.13; Copyright Power Integrations 2007	INPUT	INFO	OUTPUT	UNIT	ACDC_PeakSwitch_020107_Rev1-13.xls; PeakSwitch Continuous/Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					Customer
VACMIN	90			Volts	Minimum AC Input Voltage
VACMAX	265			Volts	Maximum AC Input Voltage
fL	50			Hertz	AC Mains Frequency
Nominal Output Voltage (VO)	12.00			Volts	Nominal Output Voltage (at continuous power)
Maximum Output Current (IO)	6.00			Amps	Power Supply Output Current (corresponding to peak power)
Minimum Output Voltage at Peak Load			12.00	Volts	Minimum Output Voltage at Peak Power (Assuming output droop during peak load)
Continuous Power	35.00		35.00	Watts	Continuous Output Power
Peak Power			72.00	Watts	Peak Output Power
n	0.68				Efficiency Estimate at output terminals and at peak load. Enter 0.7 if no better data available
Z			0.60		Loss Allocation Factor (Z = Secondary side losses / Total losses)
tC Estimate	3.00			mSeconds	Bridge Rectifier Conduction Time Estimate
CIN	180.00		180	uFarads	Input Capacitance
ENTER PeakSwitch VARIABLES					
PeakSwitch	PKS606Y		PKS606Y		PeakSwitch device
Chosen Device		*PKS606Y*			
ILIMITMIN			2.600	Amps	Minimum Current Limit
ILIMITMAX			3.000	Amps	Maximum Current Limit
fSmin			250000	Hertz	Minimum Device Switching Frequency
I^2fmin			1955	A^2kHz	I^2f (product of current limit squared and frequency is trimmed for tighter tolerance)
VOR	120.00		120	Volts	Reflected Output Voltage (VOR <= 135 V Recommended)
VDS			10	Volts	PeakSwitch on-state Drain to Source Voltage
VD			0.7	Volts	Output Winding Diode Forward Voltage Drop
VDB			0.7	Volts	Bias Winding Diode Forward Voltage Drop
VCLO			200	Volts	Nominal Clamp Voltage
KP (STEADY STATE)			0.47		Ripple to Peak Current Ratio (KP < 6)
KP (TRANSIENT)			0.29		Ripple to Peak Current Ratio under worst case at peak load (0.25 < KP < 6)
ENTER UVLO VARIABLES					
V_UV_TARGET			96	Volts	Target DC under-voltage threshold, above which the power supply with start
V_UV_ACTUAL			100	Volts	Typical DC start-up voltage based on standard value of RUV_ACTUAL
RUV_IDEAL			3.75	Mohms	Calculated value for UV Lockout resistor
RUV_ACTUAL			3.90	Mohms	Closest standard value of resistor to RUV_IDEAL
BIAS WINDING VARIABLES					
VB			15.00	Volts	Bias winding Voltage
NB			5		Number of Bias Winding Turns
PIVB			65	Volts	Bias rectifier Maximum Peak Inverse Voltage
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	EE25		EE25		User Selected Core Size(Verify acceptable thermal rise under continuous load conditions)
Core		*EE25*		*P/N:*	PC40EE25-Z
Bobbin		*EE25_BOBBIN*		*P/N:*	EE25_BOBBIN

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AE			0.404	cm^2	Core Effective Cross Sectional Area
LE			7.34	cm	Core Effective Path Length
AL			1420	nH/T^2	Ungapped Core Effective Inductance
BW			10.20	mm	Bobbin Physical Winding Width
M			0.00	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	2.00		2		Number of Primary Layers
NS	4		4		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS					
VMIN			87	Volts	Minimum DC Input Voltage
VMAX			375	Volts	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.61		Duty Ratio at full load, minimum primary inductance and minimum input voltage
IAVG			1.37	Amps	Average Primary Current
IP			2.60	Amps	Minimum Peak Primary Current
IR			1.21	Amps	Primary Ripple Current
IRMS			1.82	Amps	Primary RMS Current
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			148	uHenries	Typical Primary Inductance. +/- 12% to ensure a minimum primary inductance of 132 uH
LP_TOLERANCE			12	%	Primary inductance tolerance
NP			38		Primary Winding Number of Turns
ALG			104	nH/T^2	Gapped Core Effective Inductance
Target BM			3000	Gauss	Target Peak Flux Density at Maximum Current Limit
BM			2910	Gauss	Calculated Maximum Operating Flux Density, BM < 3000 is recommended
BAC			677	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			2053		Relative Permeability of Ungapped Core
LG			0.45	mm	Gap Length (Lg > 0.1 mm)
BWE			20.4	mm	Effective Bobbin Width
OD			0.54	mm	Maximum Primary Wire Diameter including insulation
INS			0.07	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.47	mm	Bare conductor diameter
AWG			25	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			323	Cmils	Bare conductor effective area in circular mils
CMA			177	Cmils/Amp	Primary Winding Current Capacity (100 < CMA < 500)
TRANSFORMER SECONDARY DESIGN PARAMETERS					
Lumped parameters					
ISP			24.57	Amps	Peak Secondary Current
ISRMS			13.82	Amps	Secondary RMS Current
IRIPPLE			12.45	Amps	Output Capacitor RMS Ripple Current
CMS			2763	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			15	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
VOLTAGE STRESS PARAMETERS					
VDRAIN			665	Volts	Maximum Drain Voltage Estimate (Assumes 20% zener clamp tolerance and an additional 10% temperature tolerance)
PIVS			52	Volts	Output Rectifier Maximum Peak Inverse Voltage

9 Performance Data

The measurements were made at room temperature using open frame convectional cooling and a line frequency of 60 Hz.

9.1 Efficiency

The efficiency data were obtained at an output power up to 36 W, with the output voltage set to 12 V and thus a load current of 3 A.

Percent of Full Load	Efficiency (%)	
	115 VAC	230 VAC
25	80.2	80.2
50	81.2	79.8
75	81.3	80.7
100	78.2	80.7

Table 1 – Efficiency Data.

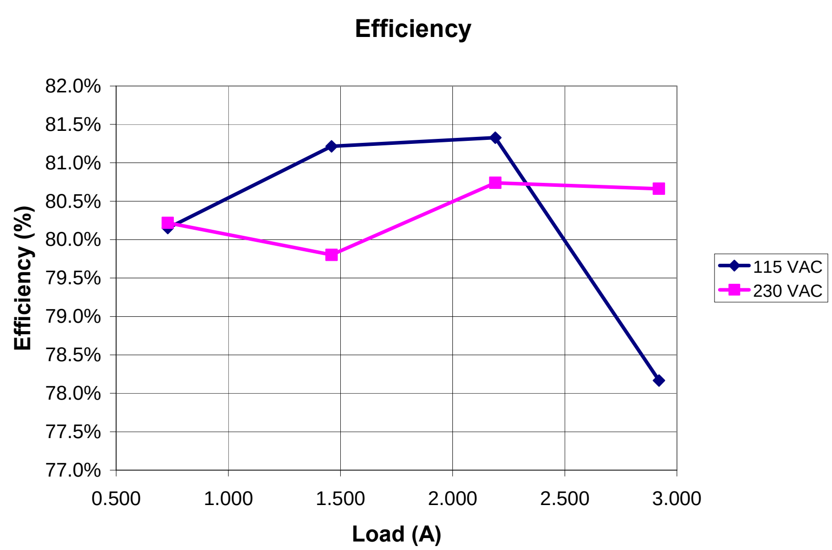

Figure 6 – Efficiency vs. Load, Room Temperature, 60 Hz.

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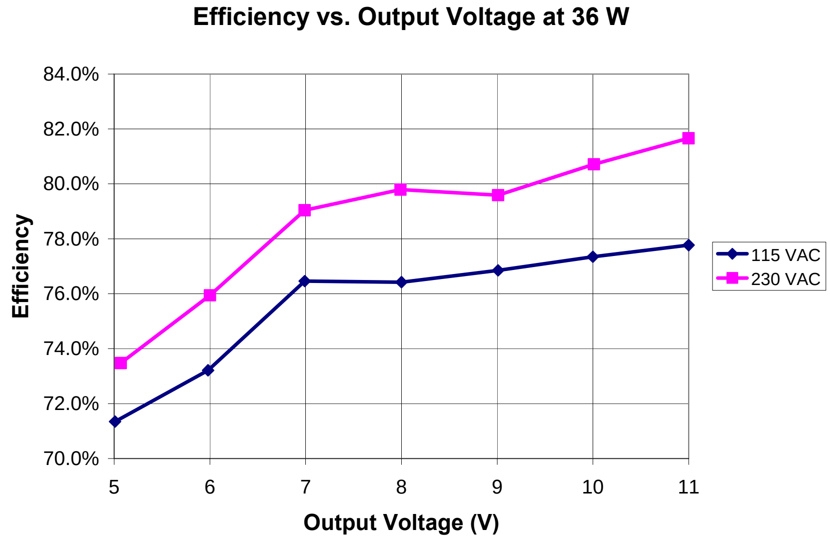

Figure 7 – Efficiency vs. Output Voltage with Full Load.

9.2 No-load Input Power

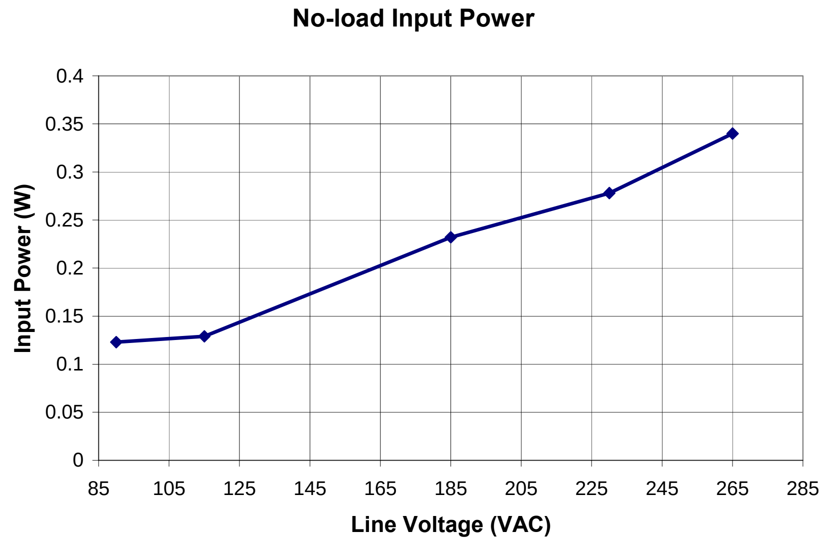

Figure 8 – Zero Load Input Power vs. Input Line Voltage, Room Temperature, 60 Hz.

9.3 Regulation

9.3.1 Load

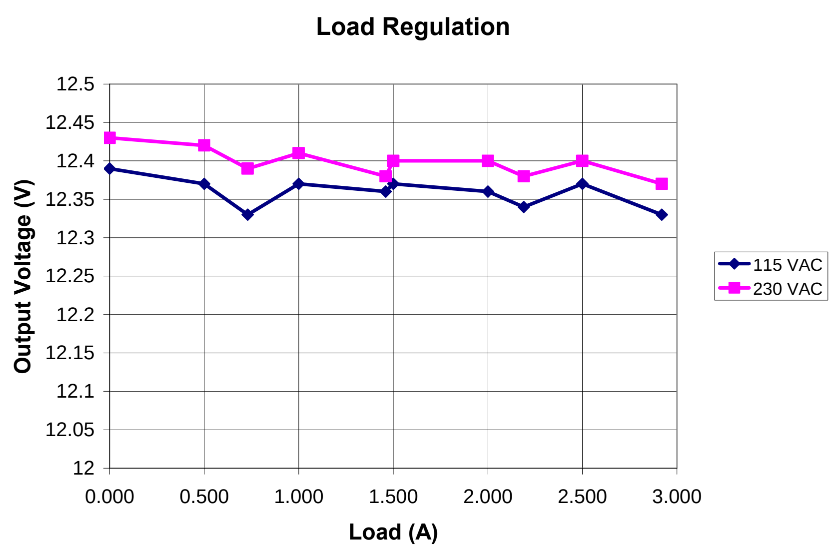

Figure 9 – Load Regulation, Room Temperature.

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9.3.2 Line

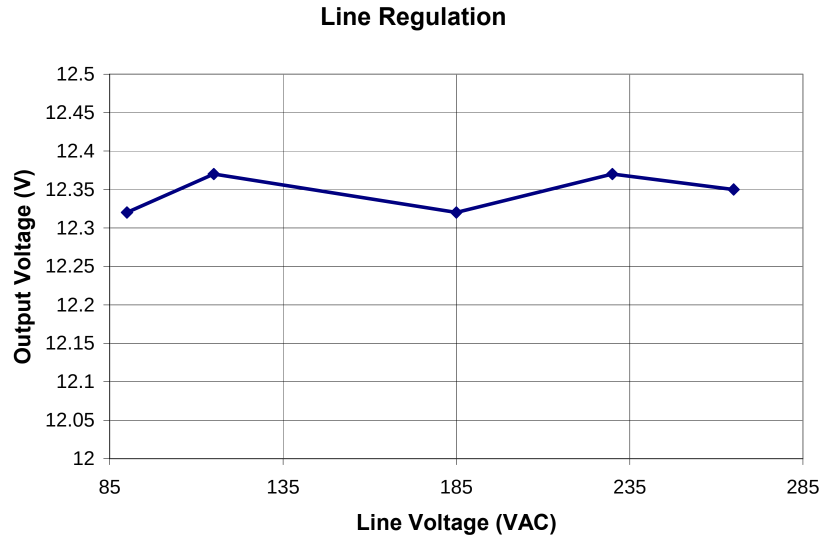

Figure 10 – Line Regulation, Room Temperature, Full Load.

9.4 Adjustable Output Voltage Characteristics

9.4.1 Resistor Control

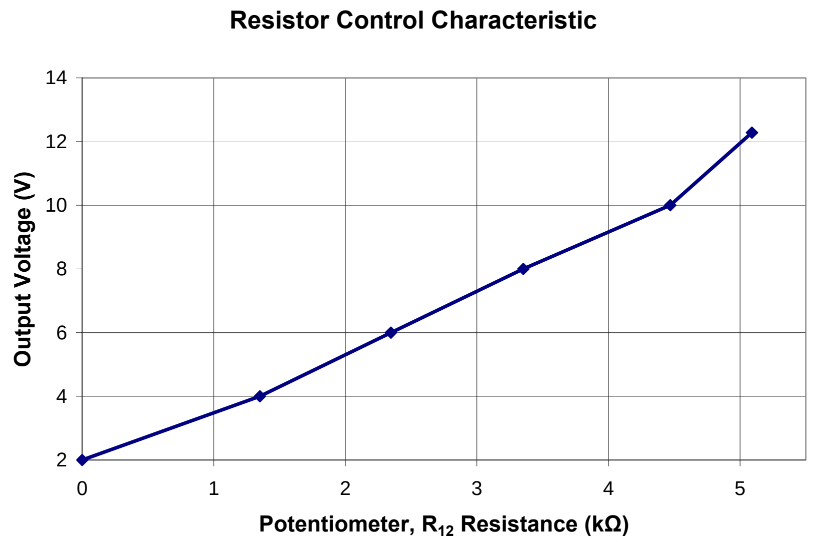

Figure 11 – Output Voltage vs. Potentiometer Resistance.

9.4.2 External Voltage Control

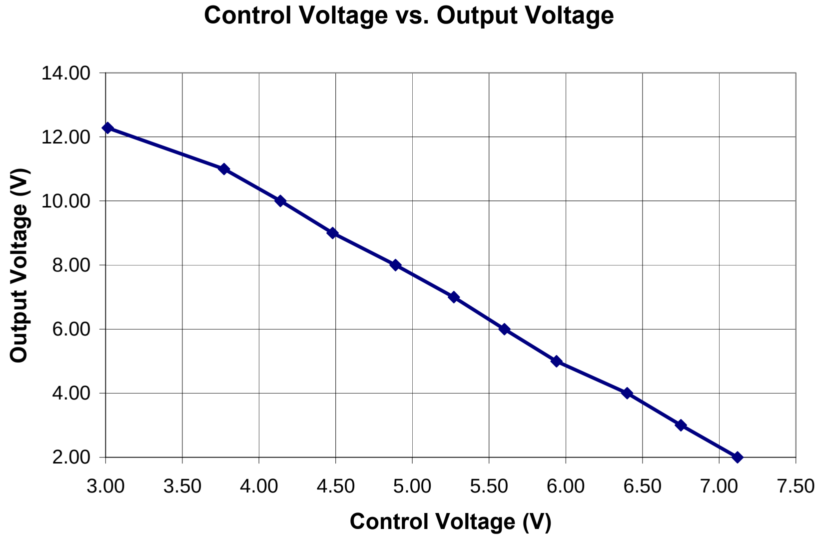

Figure 12 – Output Voltage vs. External Control Voltage.

9.5 Thermal Performance

Thermal testing of the unit was conducted in a thermal chamber under convectional cooling. The unit was placed horizontally. The volume of convectional cooling was limited by a cardboard box with dimensions 12” x 10” x 9” (Height x Width x Depth). This box was used to prevent forced air-cooling of the unit by the thermal chamber’s fan. The temperature of the *PeakSwitch* was measured by attaching a thermocouple to the device’s tab. The output diode’s temperature was monitored in an identical manner. The unit’s output voltage was approximately 12.5 V during testing with a load of 3 A.

Item	Temperature (°C)	
	90 VAC	230 VAC
Ambient	40	40
PeakSwitch, (U1)	106	100
Output Diode, (D9)	91	100
Transformer (T1)	93	94
Clamp (VR1)	115	113
Input Bridge (D1 – D4)	86	81

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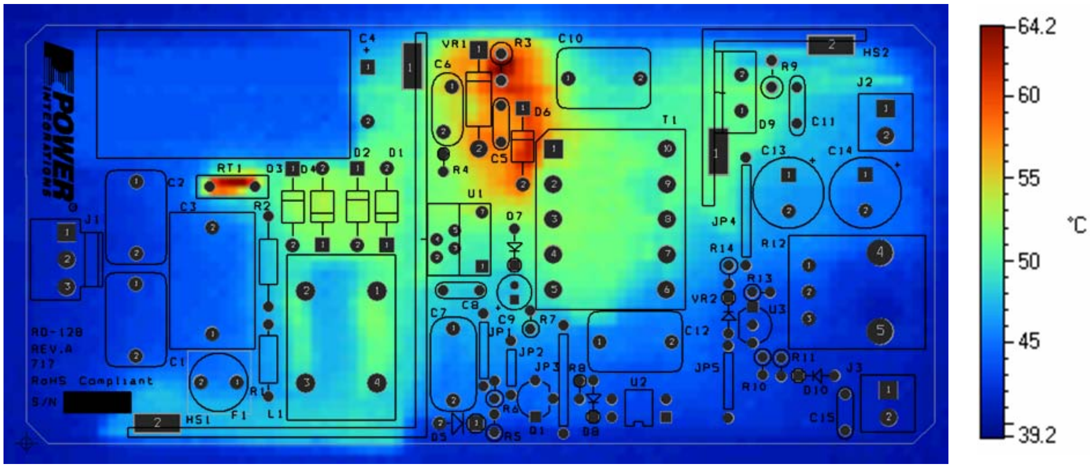

90 VAC, 36 W load, 21ºC Ambient

Figure 13 – Infrared Thermograph of Open Frame Operation at Room Temperature.

10 Waveforms

10.1 Drain Voltage and Current, Normal Operation

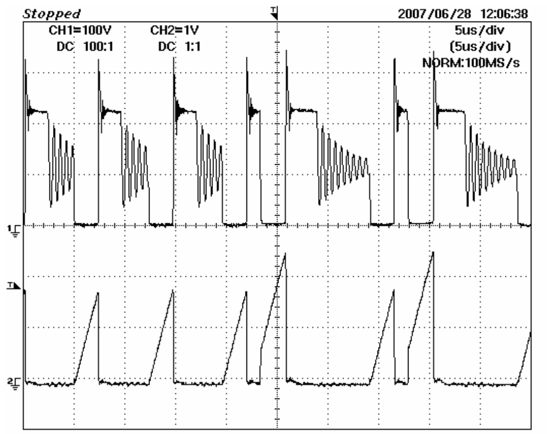

Figure 14 – 90 VAC, V_{out}= 12 V, I_o= 3 A
Upper: V_{DRAIN}, 100 V
Lower: I_{DRAIN}, 1.0 A / div, 5 µs / div.

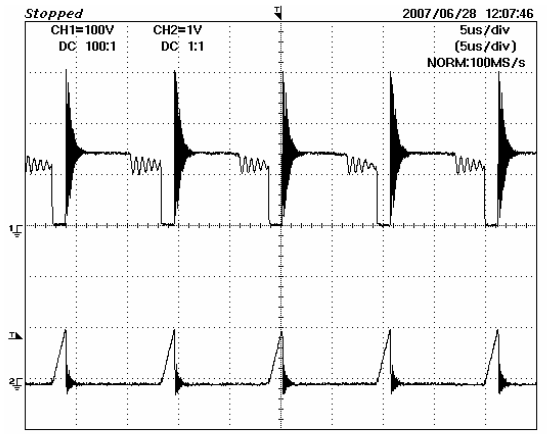

Figure 15 – 90 VAC, V_{out}= 2.3 V, I_o= 3 A
Upper: V_{DRAIN}, 100 V
Lower: I_{DRAIN}, 1.0 A / div, 5 µs / div.

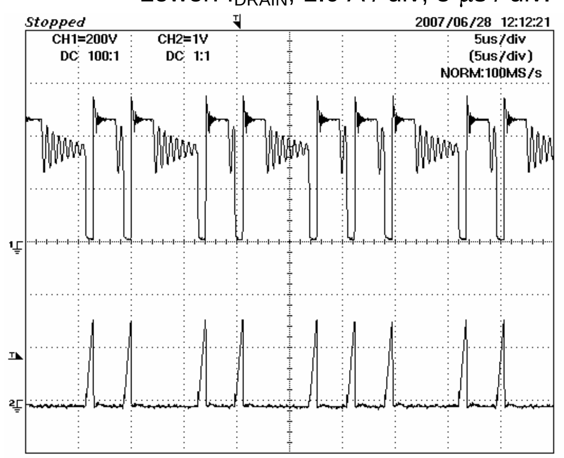

Figure 16 – 230 VAC, V_{out}= 12 V, I_o= 3 A
Upper: V_{DRAIN}, 100 V
Lower: I_{DRAIN}, 1.0 A / div, 5 µs / div.

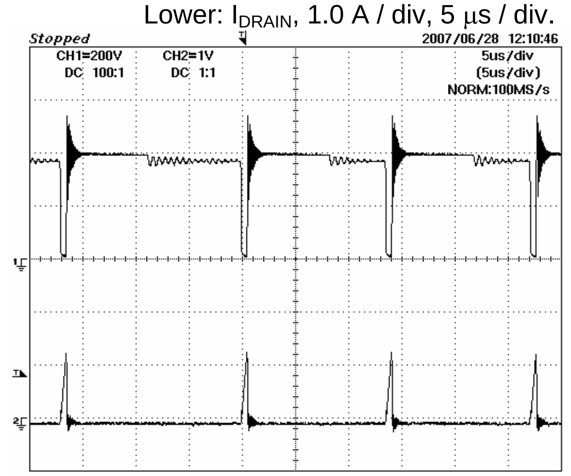

Figure 17 – 230 VAC, V_{out}= 2.3 V, I_o= 3 A
Upper: V_{DRAIN}, 100 V
Lower: I_{DRAIN}, 1.0 A / div, 5 µs / div.

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10.2 Output Voltage and Current Start-up Profile

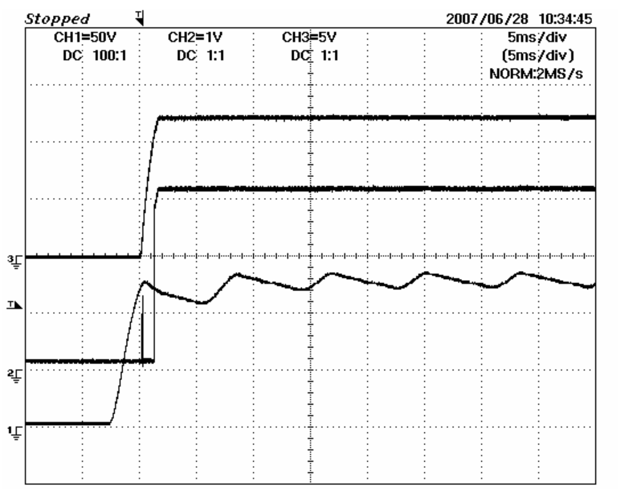

Figure 18 – Start-up Profile, 90 VAC
Upper Trace: Output Voltage 5 V / div.
Middle Trace: Output Current 1 A /div.
Lower Trace: DC Bus Voltage 50 V /div.
(Time base – 5 ms / div)

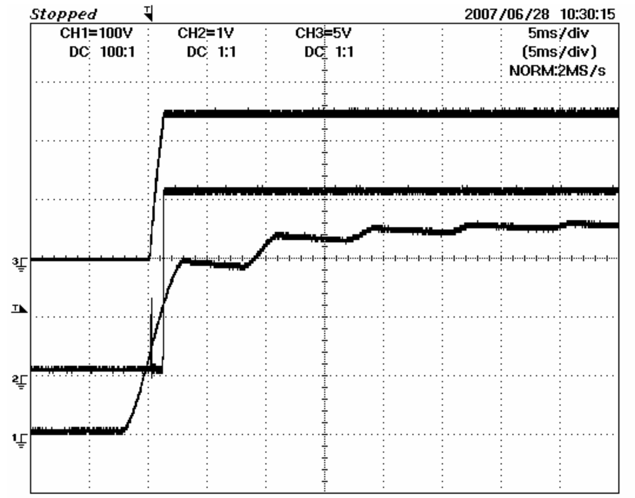

Figure 19 – Start-up Profile, 230 VAC
Upper Trace: Output Voltage 5 V / div.
Middle Trace: Output Current 1 A /div.
Lower Trace: DC Bus Voltage 100 V /div.
(Time base – 5 ms / div)

10.3 Drain Voltage and Current Start-up Profile

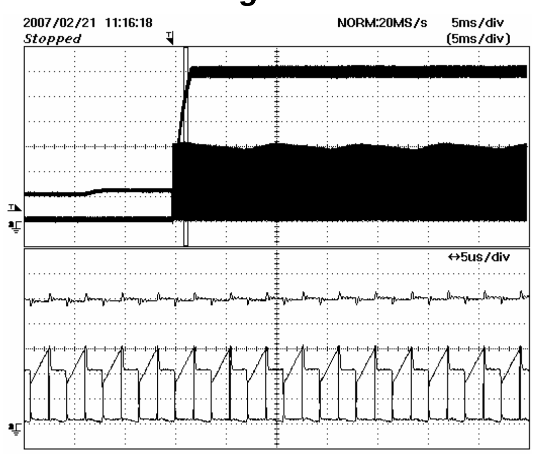

Figure 20 – 110 VAC Input
Upper: V_{out}, 2 V / div.
Middle: I_{DRAIN}, 1 A / div.
Lower: V_{DRAIN}, 100 V (5 ms / div)

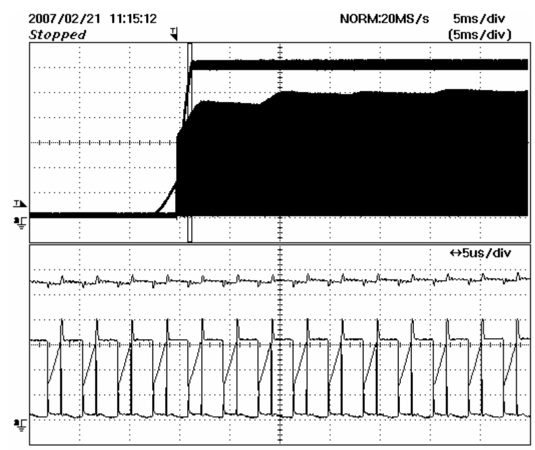

Figure 21 – 265 VAC Input and Maximum Load. Upper: V_{out}, 2 V / div.
Middle: I_{DRAIN}, 1 A / div.
Lower: V_{DRAIN}, 100 V (5 ms / div)

10.4 Transient Response

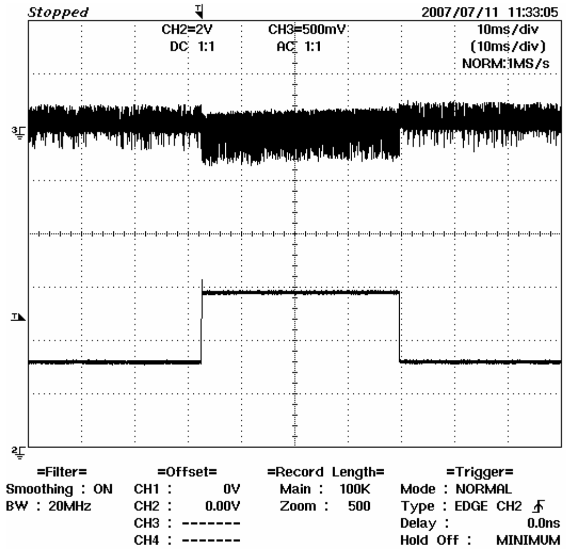

Figure 22 – 90 VAC Input
Upper: V_{out}, 500 mV / div. (AC coupled)
Lower: I_{DRAIN}, 2 A / div.
(10 ms / div)

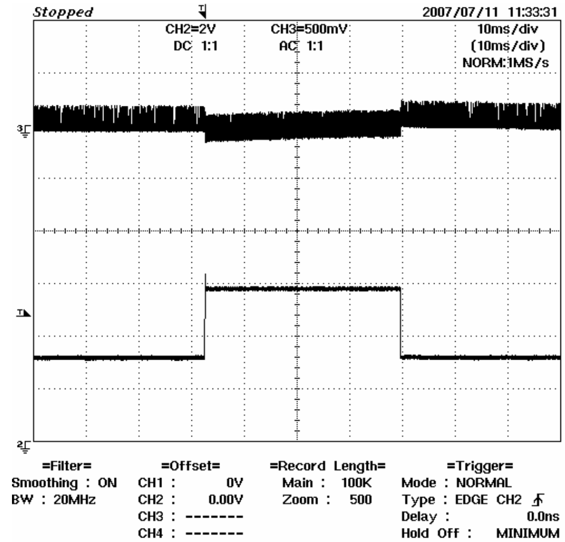

Figure 23 – 265 VAC Input and Maximum Load.
Upper: V_{out}, 500 mV / div. (AC coupled)
Lower: I_{DRAIN}, 2 A / div.
(10 ms / div)

10.5 Output Voltage and DC Bus Voltage Ripple

For this measurement the supply's full peak power was pulsed for approximately 50 ms and the DC bus voltage was measured in addition to the output voltage's ripple.

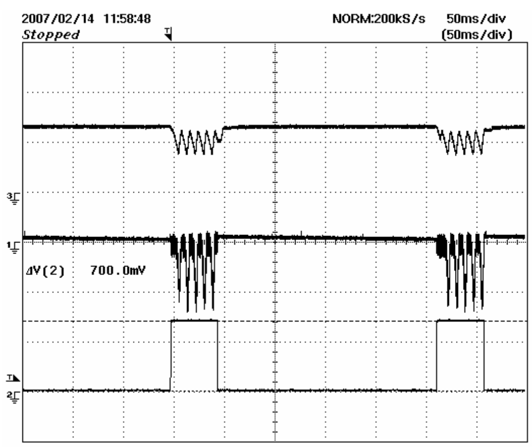

Figure 24 – 90 VAC Input, V_{out}=11 V
Upper Trace: DC Bus Voltage 100 V / div.
Middle Trace: V_{out} Ripple, 1 V / div.
Lower Trace: I_{out}=7 A
50 ms / div.

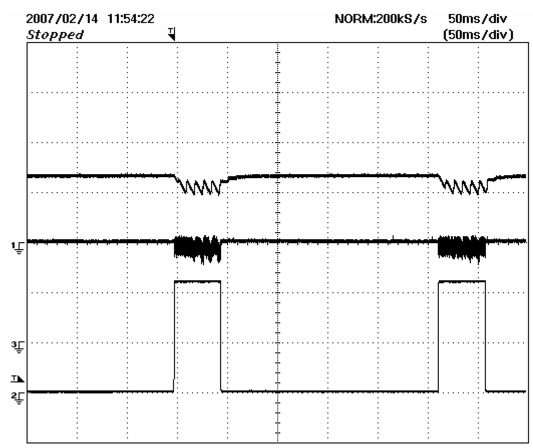

Figure 25 – 230 VAC Input, V_{out}=11 V
Upper Trace: DC Bus Voltage 100 V / div.
Middle Trace: V_{out} Ripple, 1 V / div.
Lower Trace: I_{out}=12 A
50 ms / div.

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10.6 Latching Shutdown Operation

The waveform shown below illustrates the power supply's latching shutdown feature. This feature is invaluable in a motor application due to the short circuit condition that can occur if the motor were to become jammed.

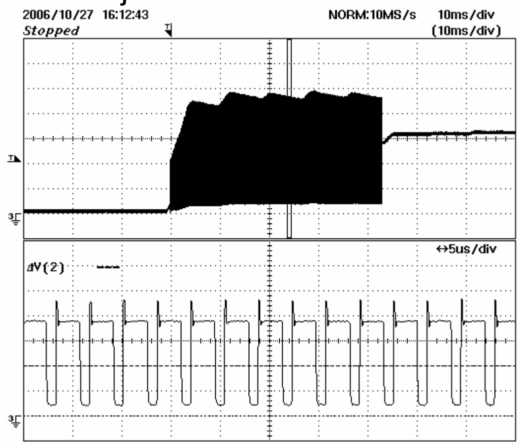

Figure 26 – Latching Shutdown Operation.

10.7 Output Ripple Measurements

10.7.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pickup. Details of the probe modification are provided in the figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 1.0 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

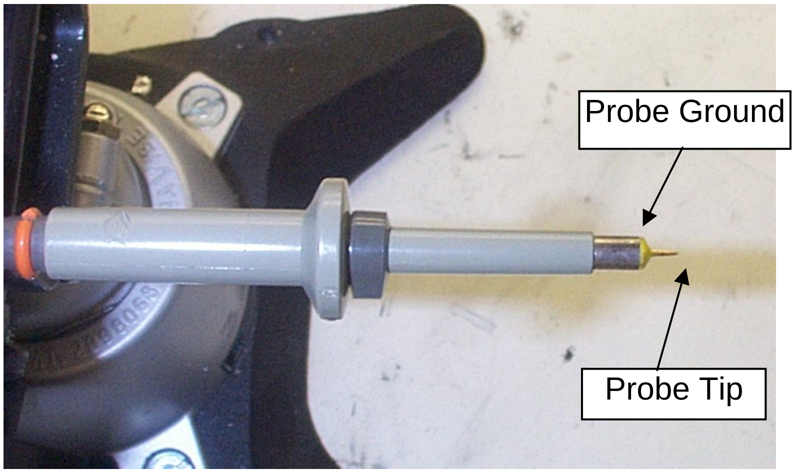

Figure 27 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

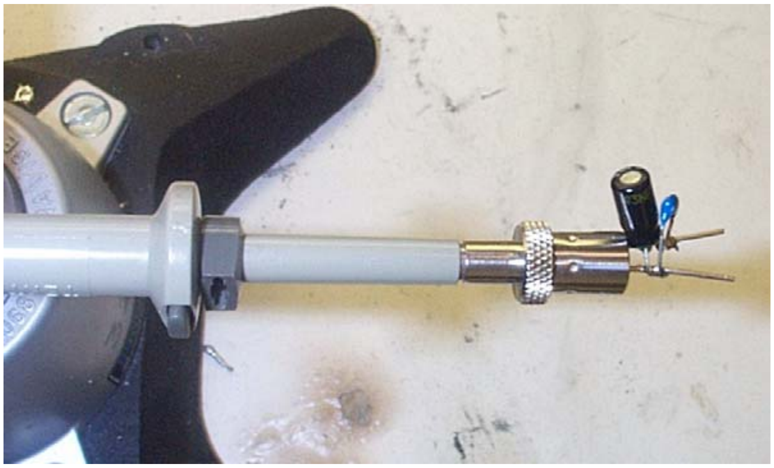

Figure 28 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement and two parallel decoupling capacitors added)

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10.7.2 Measurement Results

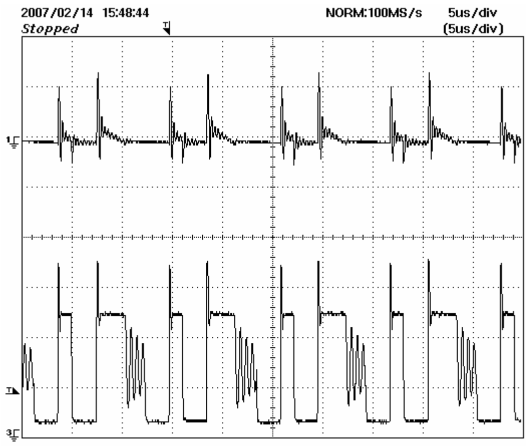

Figure 29 – 90 VAC Input, V_{out}=12 V, I_o = 3 A
Upper Trace: V_{out} Ripple, 500 mV / div.
Lower Trace: V_{Drain}, 100 V /div.
(5 µs / div)

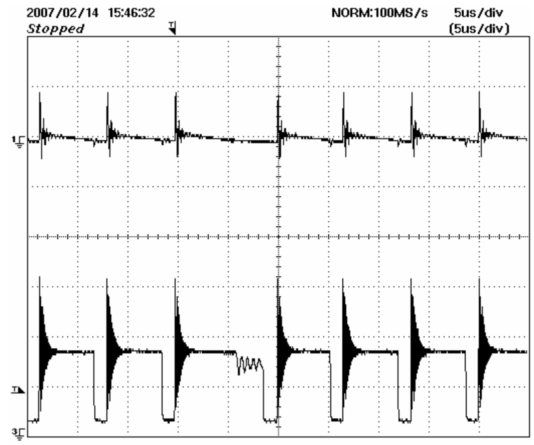

Figure 30 – 90 VAC Input, V_{out}=2.3 V, I_o = 3 A
Upper Trace: V_{out} Ripple, 500 mV / div.
Lower Trace: V_{Drain}, 100 V /div.
(5 µs / div)

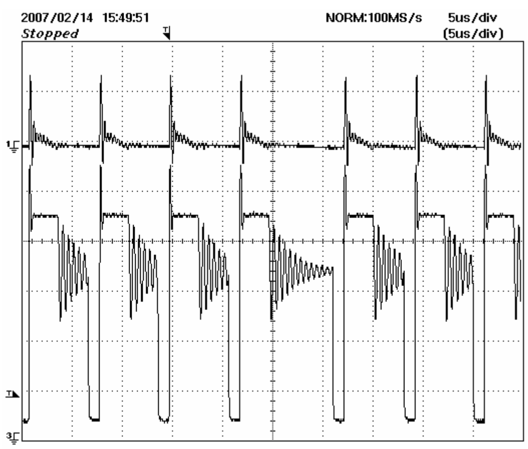

Figure 31 – 230 VAC Input, V_{out}=12 V, I_o = 3 A
Upper Trace: V_{out} Ripple, 500 mV / div.
Lower Trace: V_{Drain}, 100 V /div.
(5 µs / div)

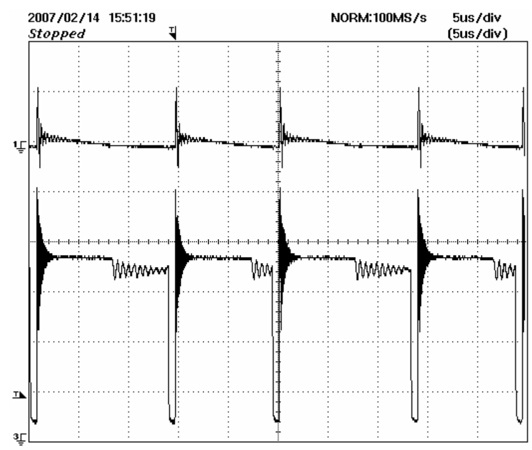

Figure 32 – 230 VAC Input, V_{out}=12 V, I_o = 3 A
Upper Trace: V_{out} Ripple, 500 mV / div.
Lower Trace: V_{Drain}, 100 V /div.
(5 µs / div)

11 Conducted EMI

The following worst case conducted EMI measurements were made with a load of 3 A with the output grounded.

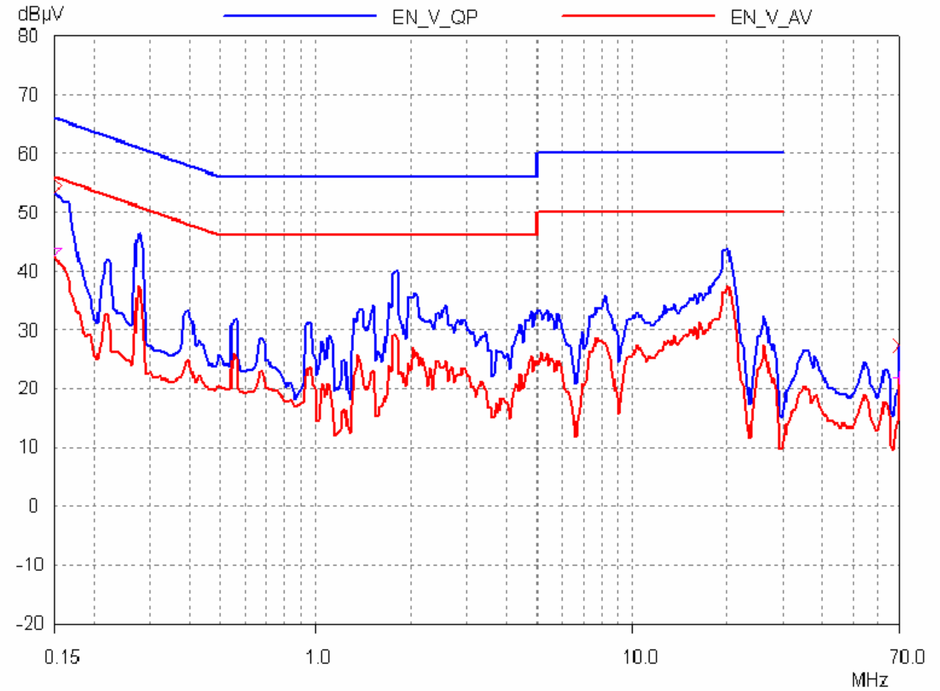

Figure 33 – Conducted EMI, Maximum Steady State Load, 90 VAC, 60 Hz, and EN55022 B Limits.

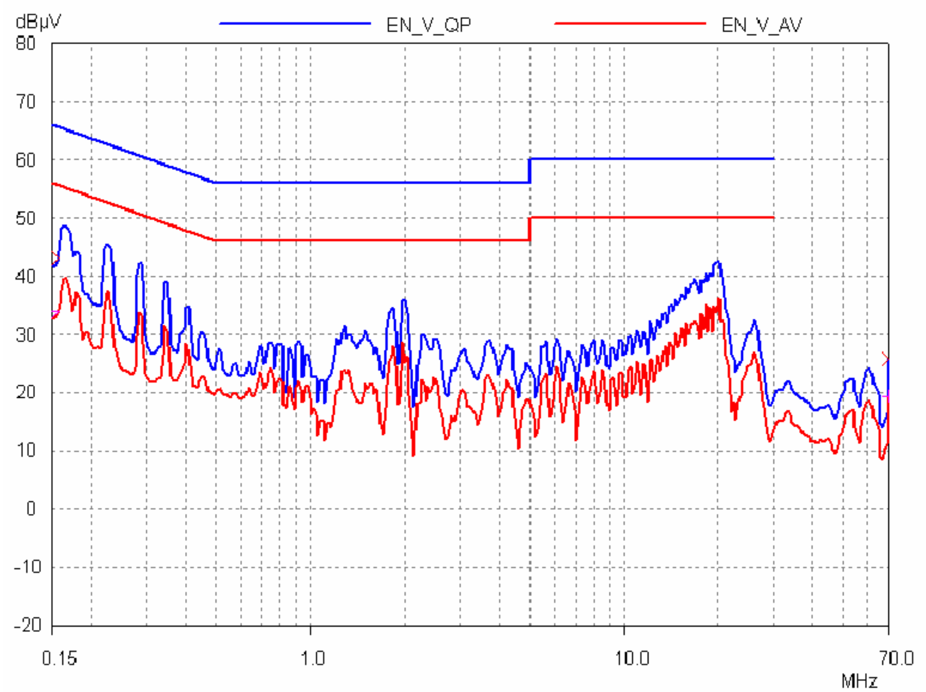

Figure 34 – Conducted EMI, Maximum Steady State Load, 230 VAC, 60 Hz, and EN55022 B Limits.

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12 Revision History

Date	Author	Revision	Description & changes	Reviewed
16-Aug-07	SK	1.0	Initial Publication	

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Notes

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The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.powerint.com. Power Integrations grants its customers a license under certain patent rights as set forth at http://www.powerint.com/ip.htm.

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