HMC743ALP6CE

v00.1212

0.5 dB LSB GaAs MMIC DUAL 6-BIT DIGITAL VARIABLE GAIN AMPLIFIER, DC - 4 GHz

Typical Applications

The HMC743ALP6CE is ideal for:

- Cellular/3G Infrastructure
- WiBro, WiMAX & LTE/4G
- Microwave Radio & VSAT
- Test Equipment and Sensors
- IF & RF Applications

Features

-45 to +18 dB Gain Control in 0.5 dB Steps

Power-up State Selection

High Output IP3: +33 dBm

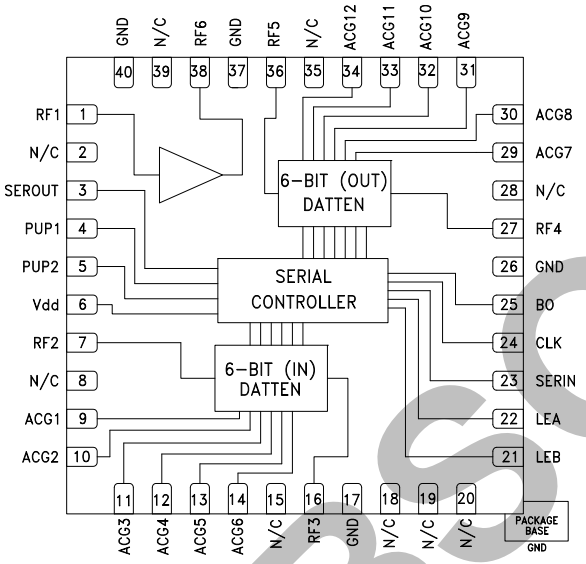
TTL/CMOS Compatible Serial Control

±0.25 dB Typical Gain Step Error

Single +5V Supply

40 Lead 6x6 mm SMT Package: 36 mm²

Functional Diagram



General Description

The HMC743ALP6CE is a digitally controlled variable gain amplifier which operates from DC to 4 GHz, can be programmed to provide 63 dB of gain control in 0.5 dB steps and delivers output IP3 of up to +33 dBm. The gain control interface accepts a three wire serial input word and allows independent or simultaneous control of two 6-bit digital attenuators. The HMC743ALP6CE also features a user selectable power up state and a serial output for cascading other serially controlled Hittite products. The HMC743ALP6CE is housed in an RoHS compliant 6x6 mm QFN leadless package, and requires minimal external components.

Electrical Specifications, T_A = +25° C, 50 Ohm System Vdd = +5V, Vcc = +5V

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency Range		70 - 1000			700 - 4000		MHz
Gain (Maximum Gain State)	15.5	18.5		6	13		dB
Gain Control Range		63			63		dB
Input Return Loss		18			19		
Output Return Loss		15			17		dB
Gain Accuracy: (Referenced to Maximum Gain State) All Gain States		70 - 350 MHz: ± (0.3 + 3.5%) 350 - 750 MHz: ± (0.3 + 5.0%) 750 - 1000 MHz: ± (0.3 + 4.0%)			0.7 - 1.7 GHz: ± (0.3 + 4.5%) 1.7 - 3.2 GHz: ± (0.3 + 4.0%) 3.2 - 4.0 GHz: ± (0.3 + 5.0%)		dB dB dB
Output Power for 1 dB Compression		17.5			17		dBm
Output Third Order Intercept Point (Two-Tone Output Power= 8 dBm Each Tone)		33			28		dBm
Noise Figure		6			7		dB
Switching Characteristics tRISE, tFall (10 / 90% RF) tON, tOFF (Latch Enable to 10 / 90% RF)		 100 160			 100 160		 ns ns
Supply Current (Idd)		5			5		mA
Supply Current (Icc)		82	102		82	102	mA

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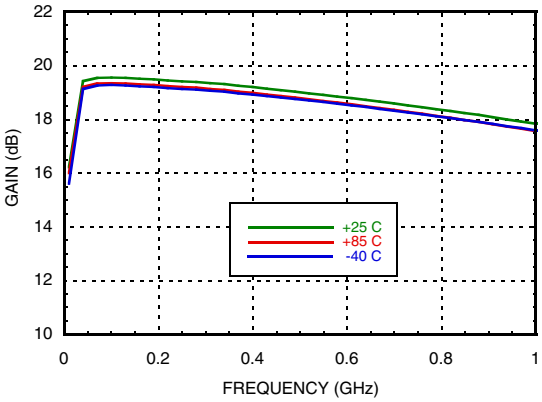
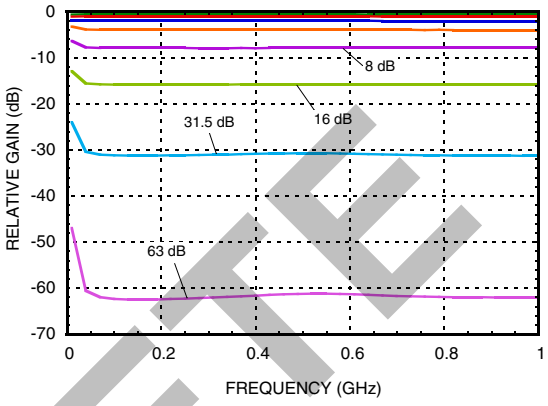
70 to 1000 MHz Tuning

Maximum Gain vs. Temperature

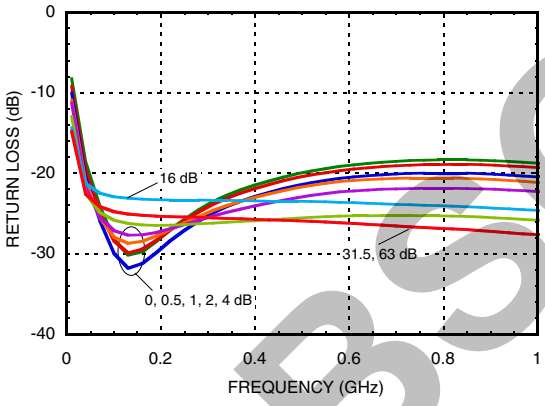


Relative Gain Setting [1]

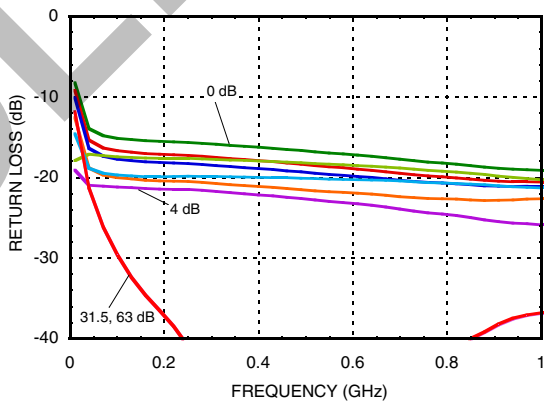
(Referenced to Maximum Gain State)



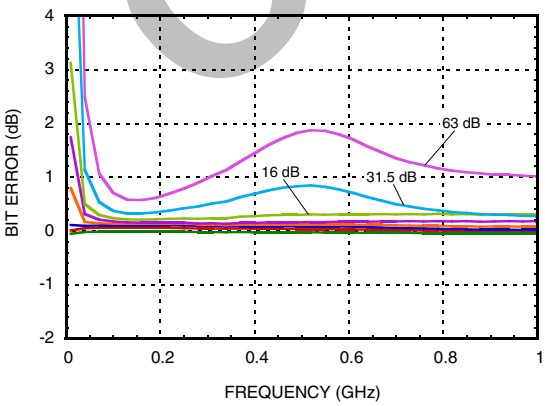
Input Return Loss [1]



Output Return Loss [1]

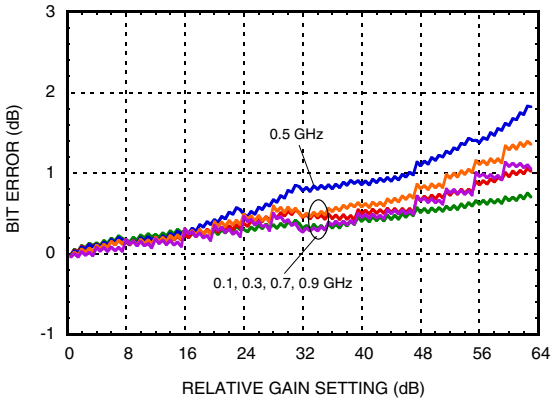


Bit Error vs. Frequency [1]



Bit Error vs. Relative Gain State [1]

(Major Frequencies)



[1] Input Attenuator swept for 0 - 31.5 dB States and Output Attenuator swept for 32 - 63 dB States

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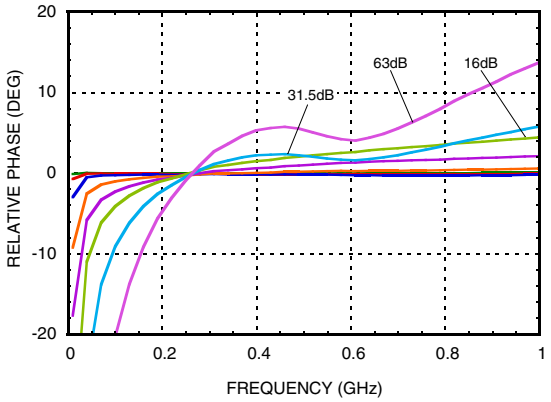
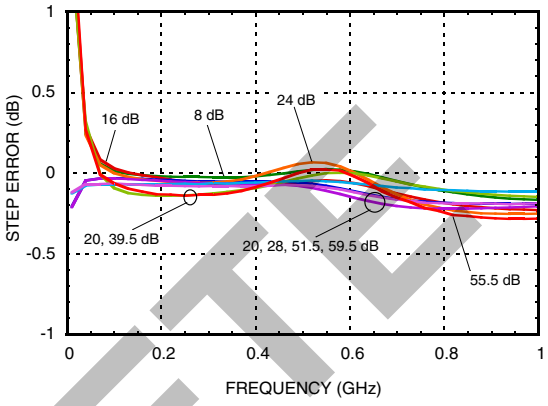
70 to 1000 MHz Tuning

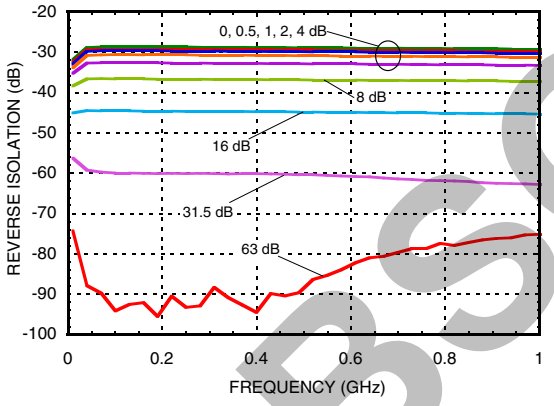
Relative Phase vs. Frequency [1]



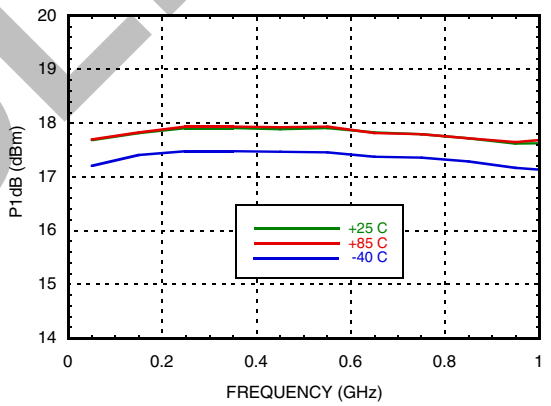
Step Error vs. Frequency [1] (Worst Case)



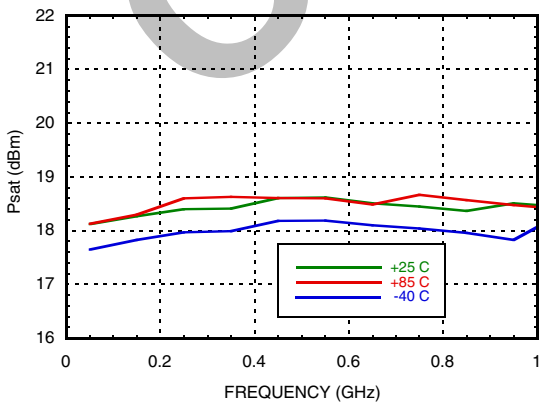
Reverse Isolation [1] (Major States)



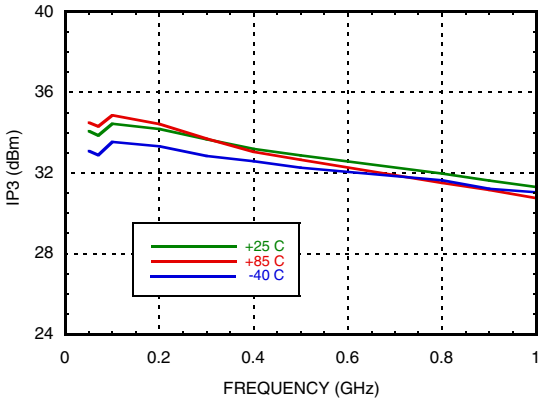
Output P1dB vs. Temperature [2]



Psat vs. Temperature [2]



Output IP3 vs. Temperature [2]



[1] Input Attenuator swept for 0 - 31.5 dB States and Output Attenuator swept for 32 - 63 dB States
[2] Max Gain State

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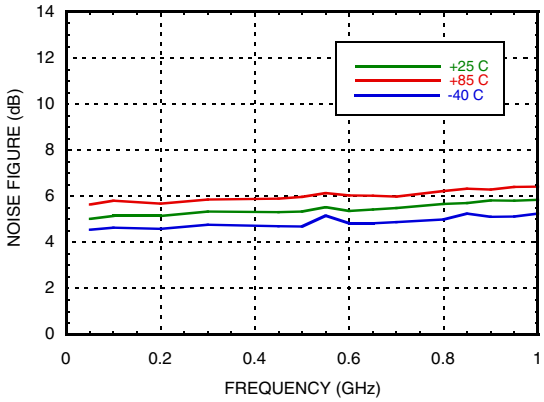
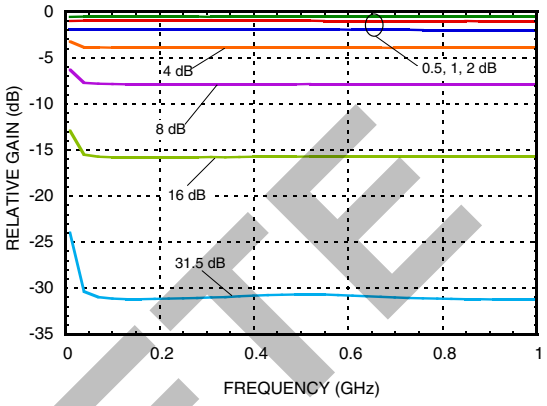
70 to 1000 MHz Tuning

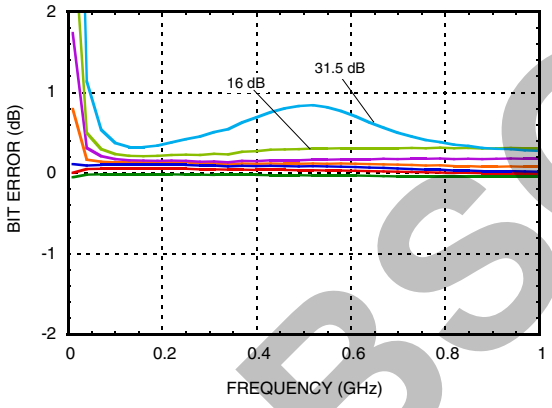
Noise Figure vs. Frequency [2]



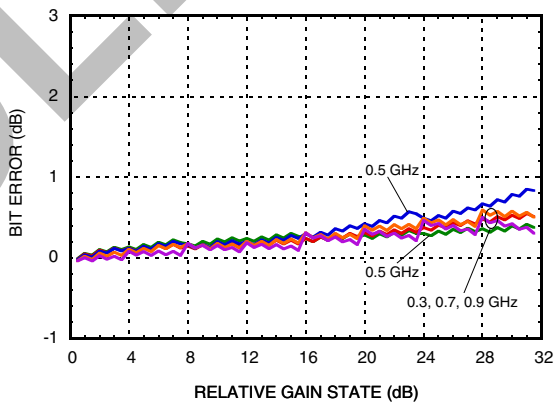
Input Attenuator Relative Attenuation [3] (Major States)



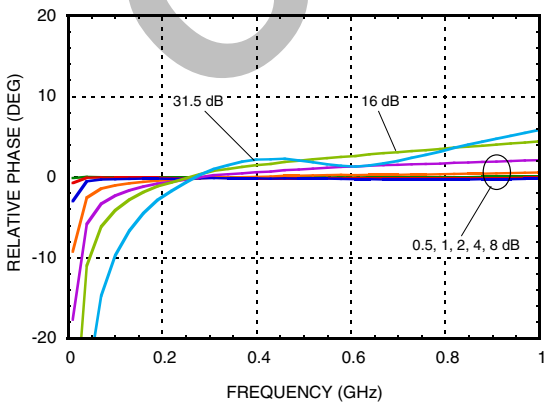
Input Attenuator Bit Error vs. Frequency [3] (Major States)



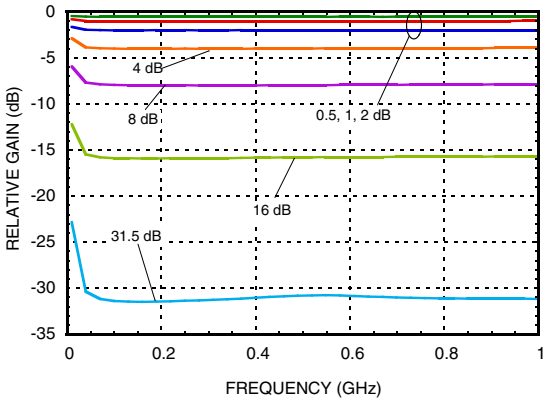
Input Attenuator Bit Error vs. Attenuation State [3] (Major Frequencies)



Input Attenuator Relative Phase vs. Frequency [3] (Major States)



Output Attenuator Relative Attenuation [4] (Major States)



[2] Max Gain State

[3] Output Attenuator set to 0 dB State

[4] Input Attenuator set to 0 dB State

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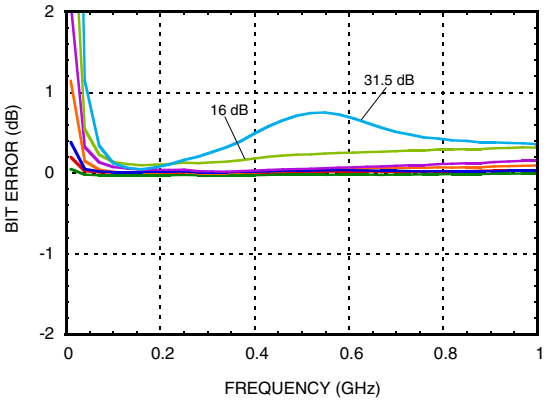
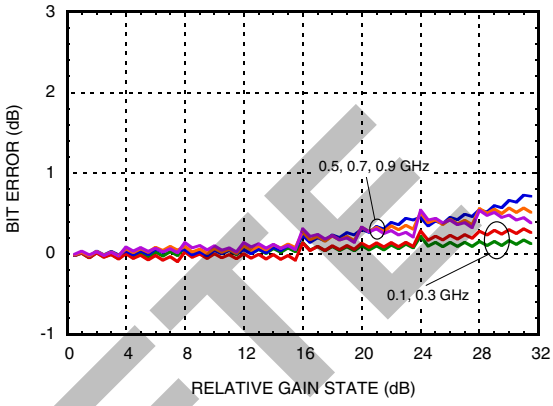
70 to 1000 MHz Tuning

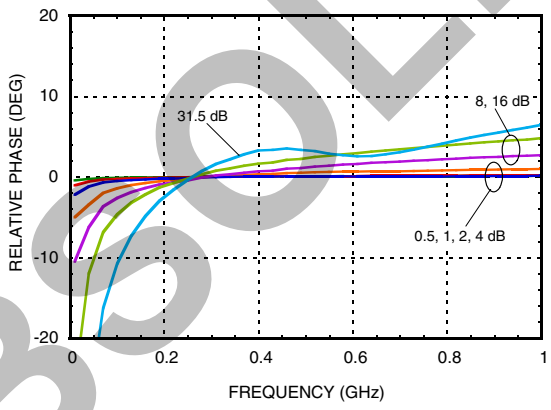
Output Attenuator Bit Error vs. Frequency [4] (Major States)



Output Attenuator Bit Error vs. Attenuation State [4] (Major Frequencies)



Output Attenuator Relative Phase vs. Frequency [4] (Major States)



[4] Input Attenuator set at 0 dB State

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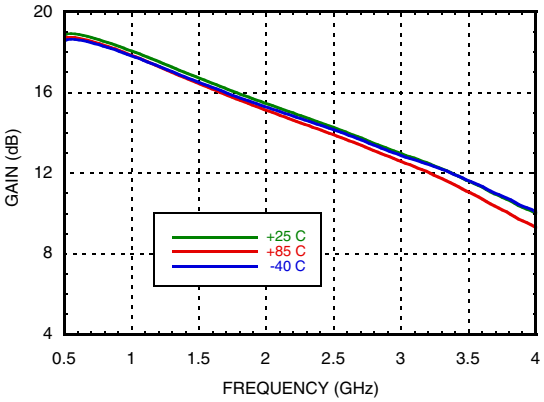
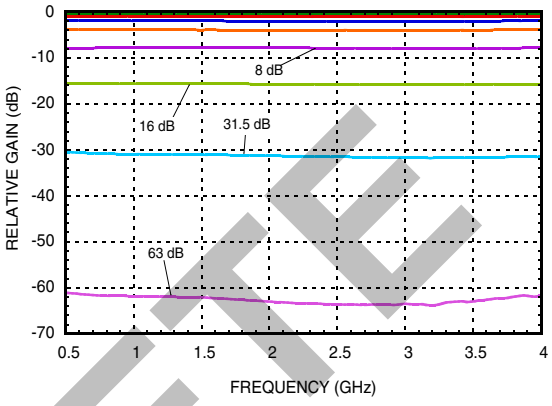
0.7 to 4.0 GHz Tuning

Maximum Gain vs. Temperature

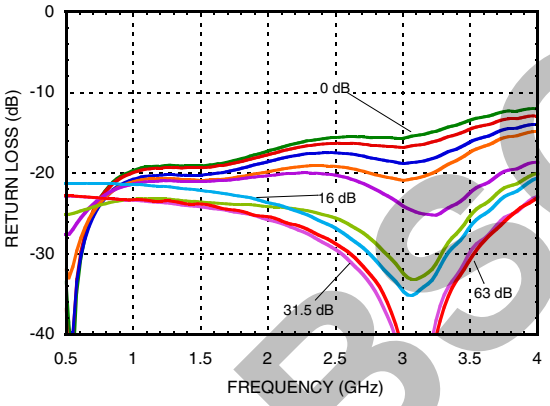


Relative Gain Setting [1]

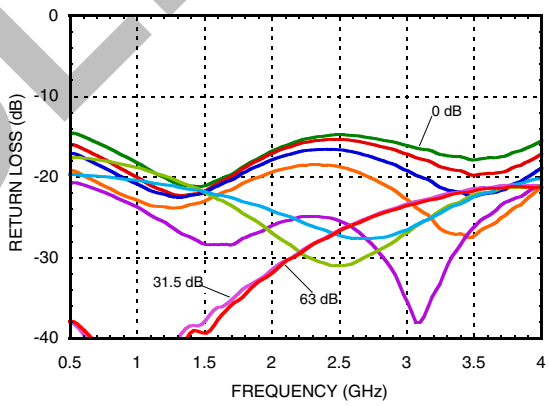
(Referenced to Maximum Gain State)



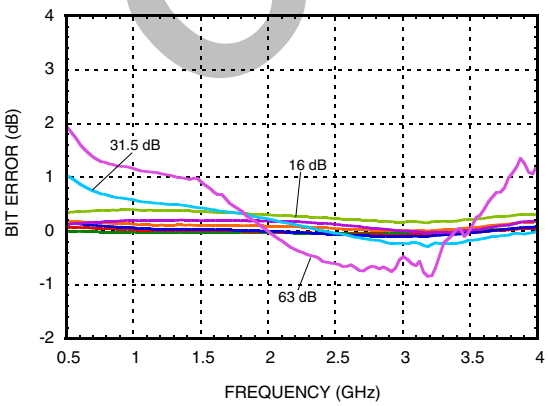
Input Return Loss [1]



Output Return Loss [1]

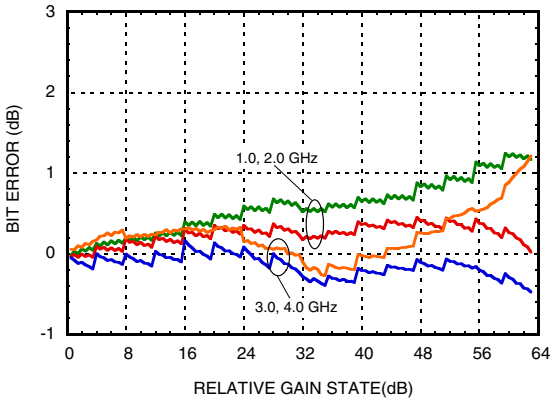


Bit Error vs. Frequency [1]



Bit Error vs. Relative Gain State [1]

(Major Frequencies)



[1] Input Attenuator swept for 0 - 31.5 dB States and Output Attenuator swept for 32 - 63 dB States

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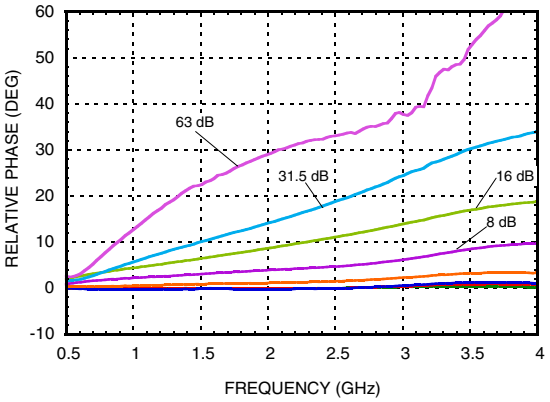
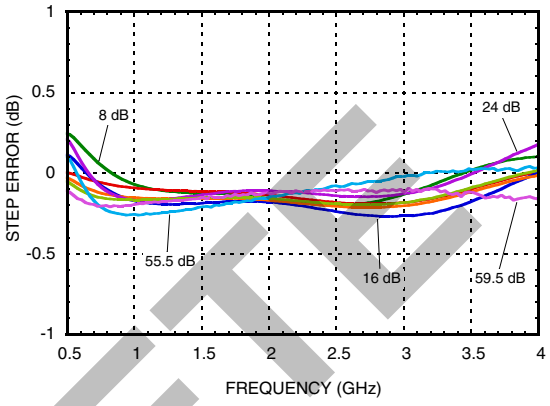
0.7 to 4.0 GHz Tuning

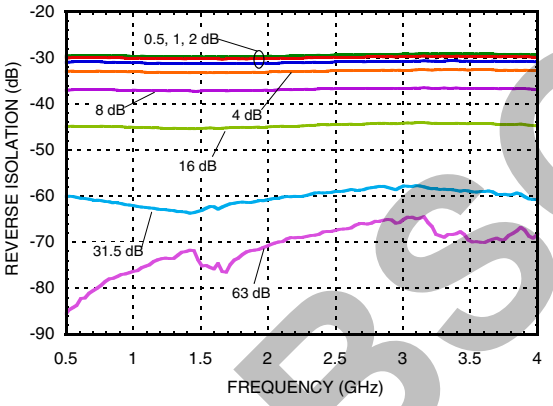
Relative Phase vs. Frequency [1]



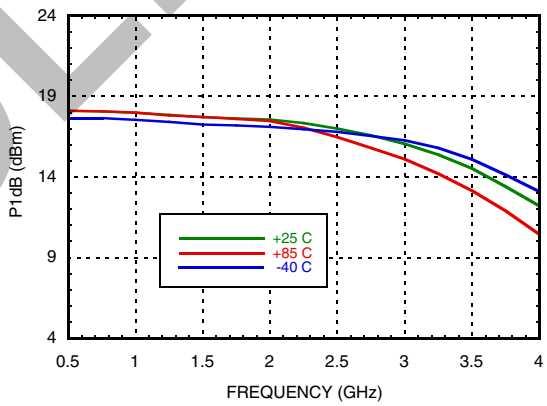
Step Error vs. Frequency (Worst Case) [1]



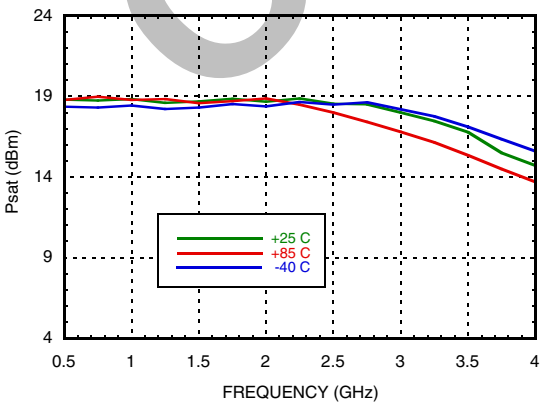
Reverse Isolation [1]



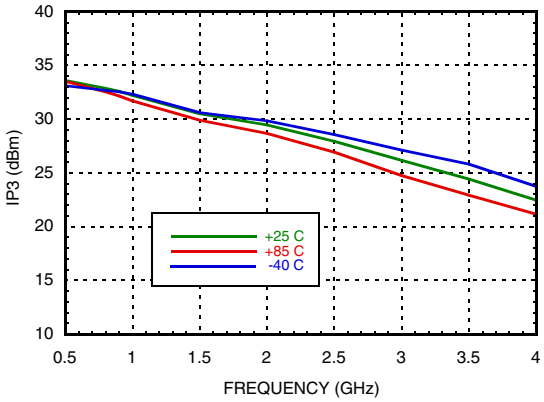
Output P1dB vs. Temperature [2]



Psat vs. Temperature [2]



Output IP3 vs. Temperature [2]



[1] Input Attenuator swept for 0 - 31.5 dB States and Output Attenuator swept for 32 - 63 dB States
[2] Max Gain State

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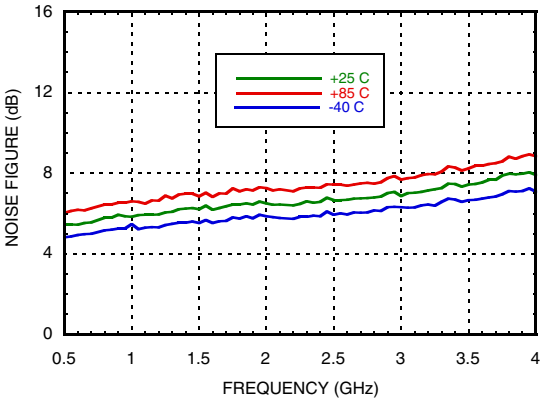
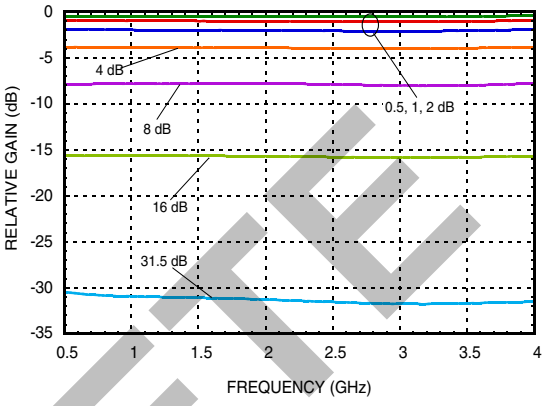
0.7 to 4.0 GHz Tuning

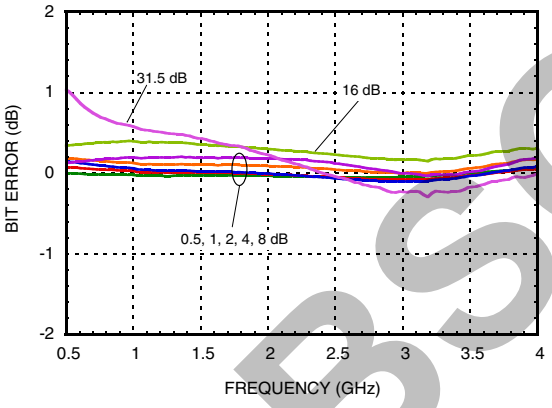
Noise Figure vs. Frequency [2]



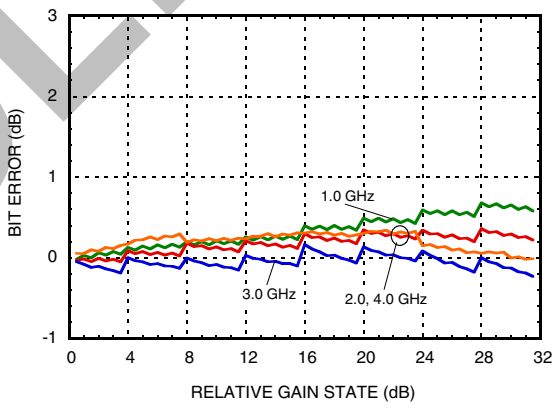
Input Attenuator Relative Attenuation [3] (Major States)



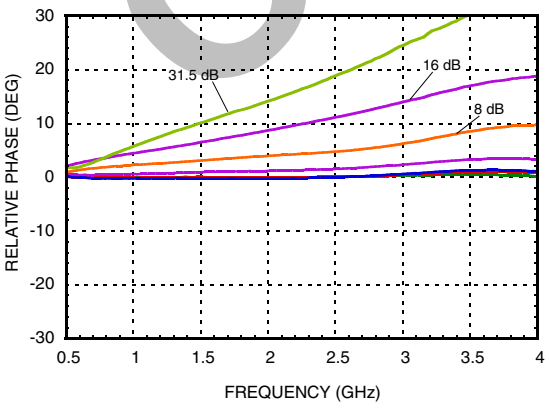
Input Attenuator Bit Error vs. Frequency [3] (Major States)



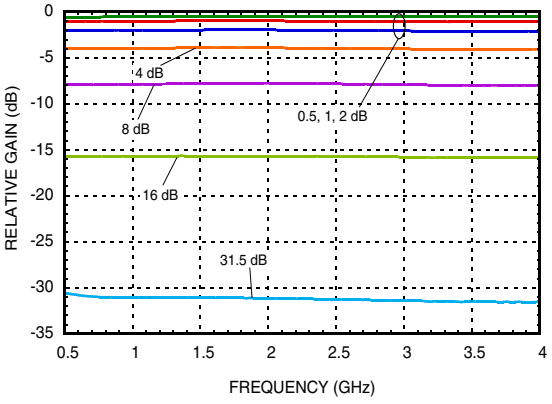
Input Attenuator Bit Error vs. Attenuation State [3] (Major Frequencies)



Input Attenuator Relative Phase vs. Frequency [3] (Major States)



Output Attenuator Relative Attenuation [4] (Major Steps)



[2] Max Gain State

[3] Output Attenuator set to 0 dB Stat

[4] Input Attenuator set to 0 dB State

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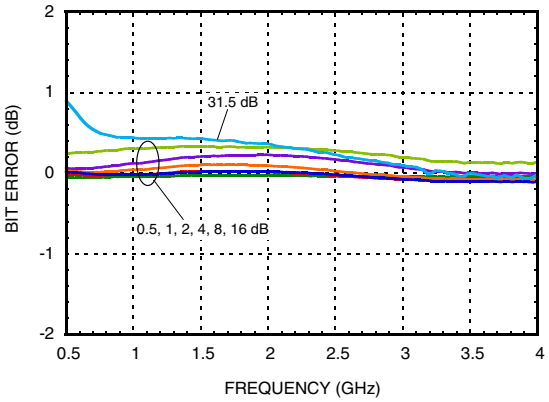
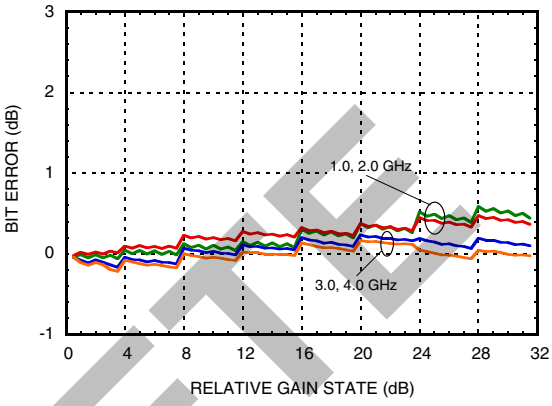
0.7 to 4.0 GHz Tuning

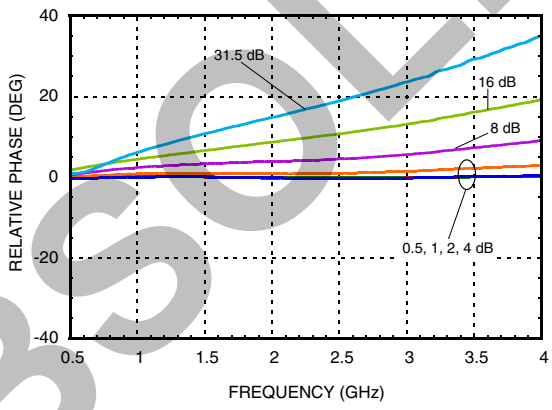
Output Attenuator Bit Error vs. Frequency [4] (Major States)



Output Attenuator Bit Error vs. Attenuation State [4] (Major Frequencies)



Output Attenuator Relative Phase vs. Frequency [4] (Major States)



[4] Input Attenuator set at 0 dB State

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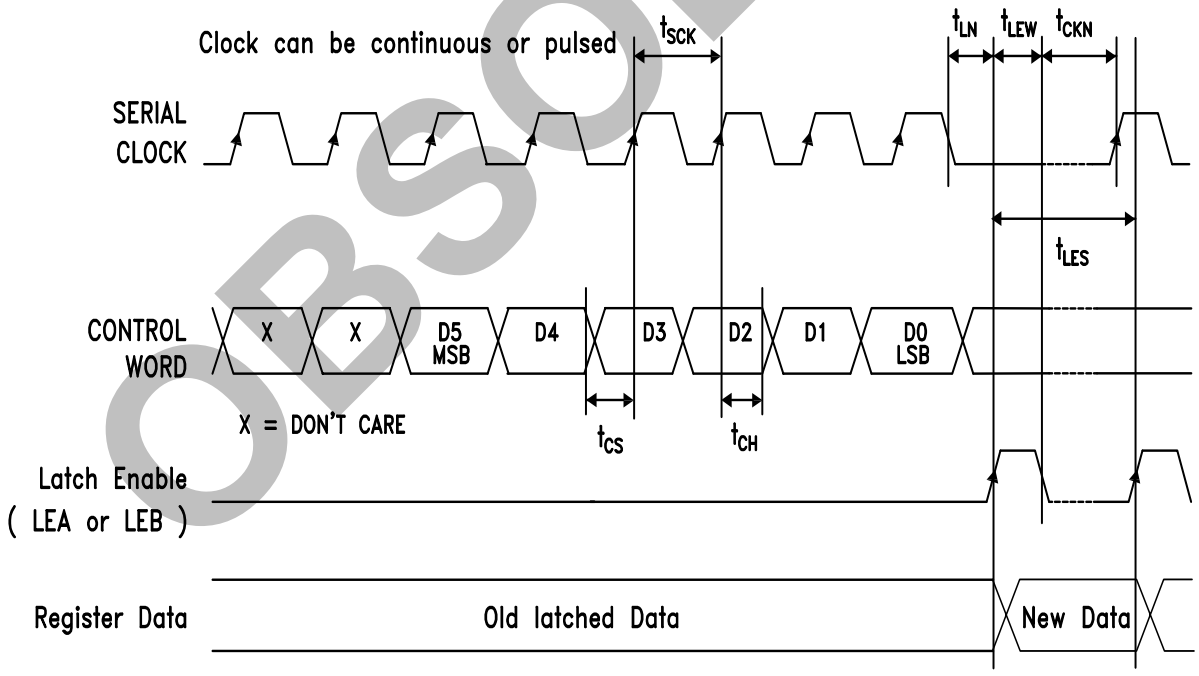
Serial Control Interface

The HMC743ALP6CE contains a 3-wire SPI compatible digital interface (SERIN, CLK, LEA or LEB and BO) to control 8-bit word serial data. The input (IN) and output (OUT) attenuators can be individually controlled via the latch enable pins. The LEA pin latches the serial 8-bit word to the output attenuator. The LEB pin latches the serial 8-bit word to the input attenuator.

The HMC743ALP6CE can be serially controlled in one of two user-selectable modes: most significant bit first (MSB-first), or least significant bit first (LSB-first). The serial data order is selected by control input BO (bit order select). BO = HIGH sets the MSB-first mode and the BO = LOW sets the LSB-first mode. After the 8-bit serial data is clocked in, the latch enable (LEA,LEB) is pulsed to set the state of attenuator(s) according to the truth table. The input and output attenuators can be controlled independently by applying this procedure separately for each attenuator and using the correct latch enable(LEA or LEB) , or a single control word can set both attenuators by first clocking in the 8-bit serial data word, then applying latch enable pulses to LEA and LEB, either one by one or simultaneously to change the content of the registers.

MSB-First timing diagram (BO = HIGH)



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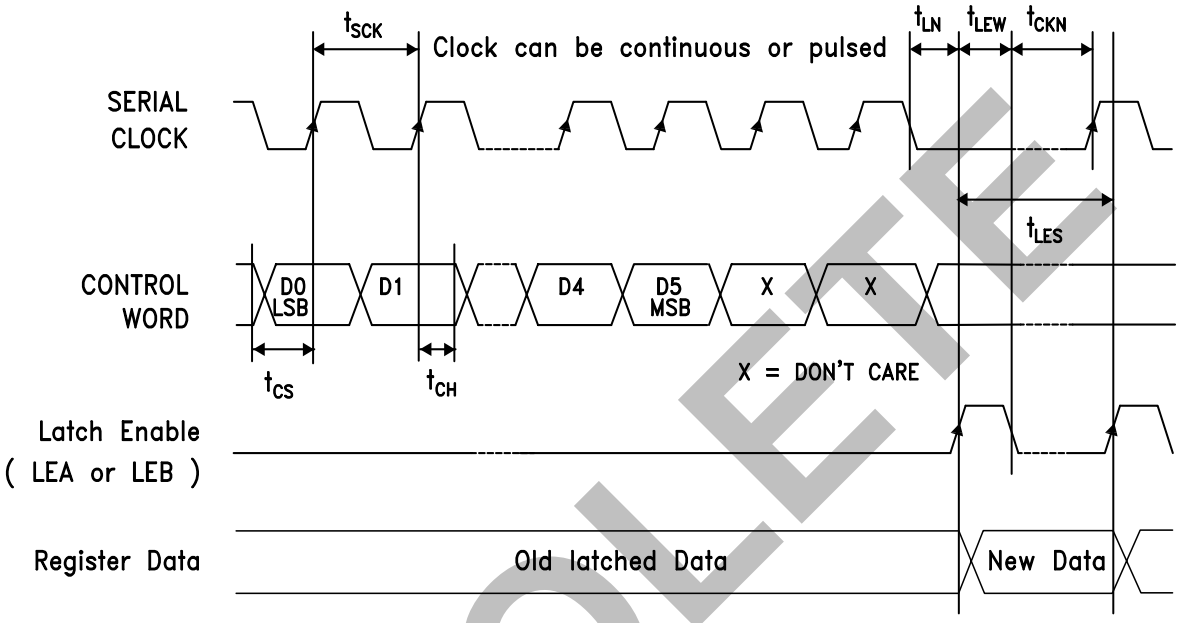
LSB-First timing diagram (BO = LOW)



Truth Table *(for each attenuator)*

Control Voltage Input						Attenuation
D5	D4	D3	D2	D1	D0	
High	High	High	High	High	High	0 dB
High	High	High	High	High	Low	-0.5 dB
High	High	High	High	Low	High	-1 dB
High	High	High	Low	High	High	-2 dB
High	High	Low	High	High	High	-4 dB
High	Low	High	High	High	High	-8 dB
Low	High	High	High	High	High	-16 dB
Low	Low	Low	Low	Low	Low	-31.5 dB
Any combination of the above states will provide an attenuation approximately equal to the sum of the bits selected.						

PUP Truth Table

LE (A and B)	PUP1	PUP2	Gain Relative to Max Setting
0	0	0	-63 dB
0	1	1	0 dB

Bit order select

	MSB-first	LSB-first
BO	1	0

Parameter	Typ.
Min. serial period, t_{SCK}	100 ns
Control set-up time, t_{CS}	20 ns
Control hold-time, t_{CH}	20 ns
LE setup-time, t_{LN}	10 ns
Min. LE pulse width, t_{LEW}	10 ns
Min LE pulse spacing, t_{LES}	630 ns
Serial clock hold-time from LE, t_{CKN}	10 ns

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Absolute Maximum Ratings

RF Input Power [1]	11.5 dBm (T = +85 °C)
Digital Inputs (CLK, LEA, LEB, SERIN, PUP1, PUP2 & B0)	-0.5V to Vdd +0.5V
Bias Voltage (Vdd)	5.6V
Collector Bias Voltage (Vcc)	5.5V
Channel Temperature	150 °C
Continuous Pdiss (T = 85 °C) (derate 8.4 mW/°C above 85 °C) [2]	0.546 W
Thermal Resistance [3]	119 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1A

[1] The maximum RF input power increases by the same amount the gain is reduced by the input attenuator. The maximum input power at any state is no more than 28 dBm.

[2] This value is the total power dissipation in the amplifier.

[3] This is the thermal resistance for the amplifier.

Control Voltage Table

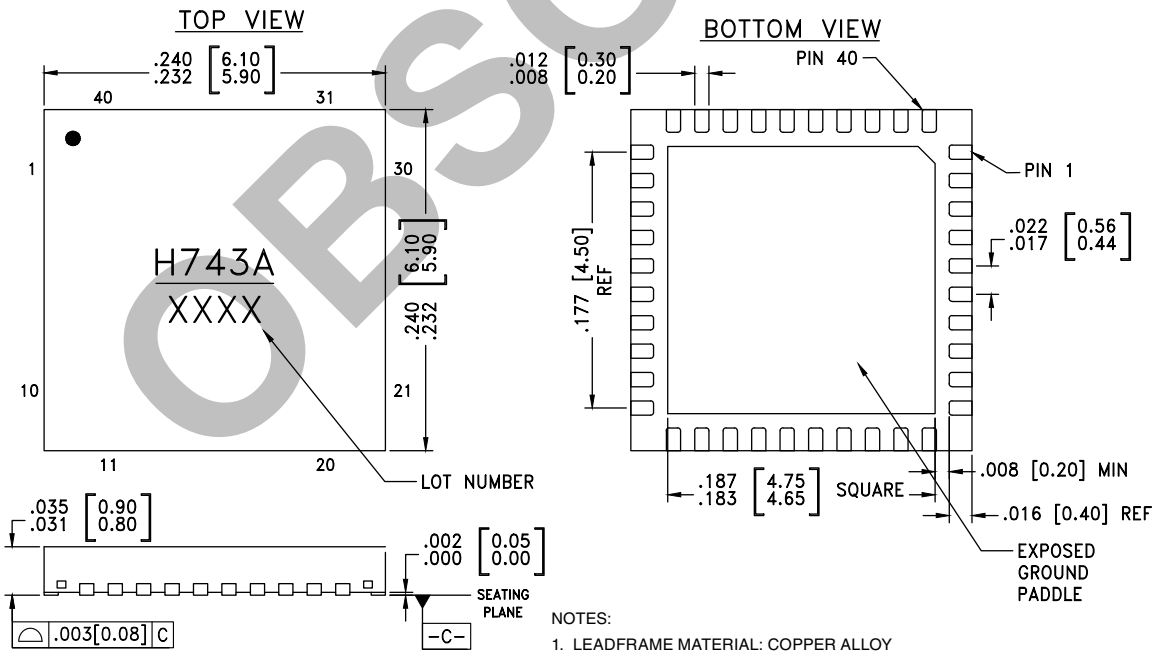
State	Vdd = +3V , Vcc = + 5V	Vdd = Vcc = +5V
Low	0 to 0.5V @ <1 µA	0 to 0.8V @ <1 µA
High	2 to 3V @ <1 µA	2 to 5V @ <1 µA

Bias Voltage

	Voltage (V)	Current (Typ.) (mA)
Vdd	+ 3.0	4
	+ 5.0	5
Vcc	+ 5.0	82

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

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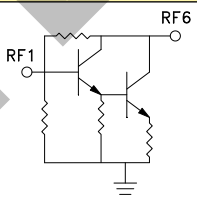
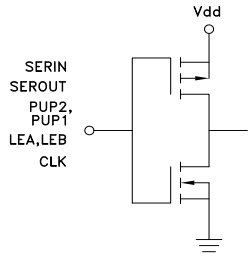
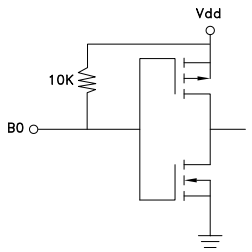
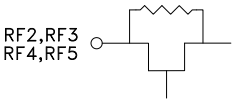
Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [2]
HMC743ALP6CE	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [1]	H743A XXXX

[1] Max peak reflow temperature of 260 °C
[2] 4-Digit lot number XXXX

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1	RF1	This pin is DC coupled. An off chip DC blocking capacitor is required.	
38	RF6	RF output and DC bias for the output stage of the amplifier.	
2, 8, 15, 18 - 20, 28, 35, 39	N/C	No Connection	
3, 23	SEROUT, SERIN	Data in and out pins	
4, 5	PUP1, PUP2	Controls power up state	
21, 22	LEB, LEA	LEA is the latch enable for the output attenuator. LEB is the latch enable for the input attenuator.	
24	CLK	Clock input	
25	BO	Controls bit order of control word. B0 - High = MSB first B0 - Low = LSB first	
6	Vdd	Supply Voltage	
7, 16, 27, 36	RF2, RF3, RF4, RF5	These pins are DC coupled and matched to 50 Ohms. Blocking capacitors are required. Select value based on lowest frequency of operation.	
9 - 14	ACG1 - ACG6	External capacitors to ground are required. Place capacitor as close to pins as possible. See “Components for Selected Frequencies” table.	
17, 26, 37, 40 Paddle	GND	These pins and the exposed ground paddle must be connected to RF/DC ground.	
29 - 34	ACG7 - ACG12	External capacitors to ground are required. Place capacitor as close to pins as possible. See “Components for Selected Frequencies” table.	

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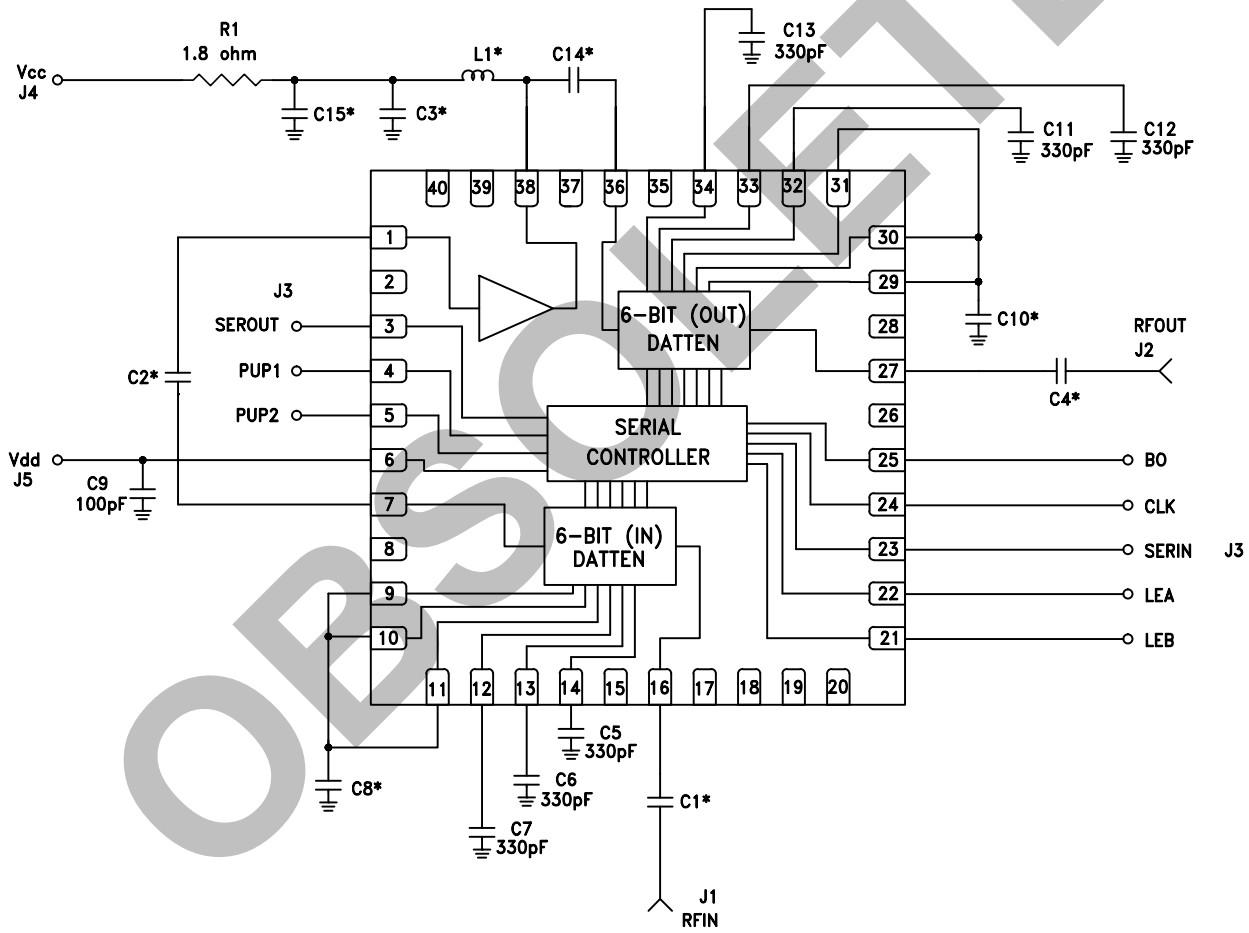
Power-Up States

The HMC743ALP6CE offers two different power up states, either full attenuation or maximum gain mode. See PUP truth table.

Power-On Sequence

The ideal power-up sequence is: GND, Vdd, digital inputs, RF inputs. The relative order of the digital inputs are not important as long as they are powered after Vdd / GND

Application Circuit



Components for Selected Frequencies *

Tuned Frequency	70 - 1000 MHz	700 - 4000 MHz
Evaluation PCB	124459 - HMC743ALP6C [1]	124460 - HMC743ALP6C [1]
C3 (pF)	1000	100
C1, C2, C4, C14 (pF)	3300	100
C8, C10 (pF)	100	330
C15 (pF)	2200	1000
L1 (nH)	560	36

[1] Reference this number when ordering complete evaluation PCB.

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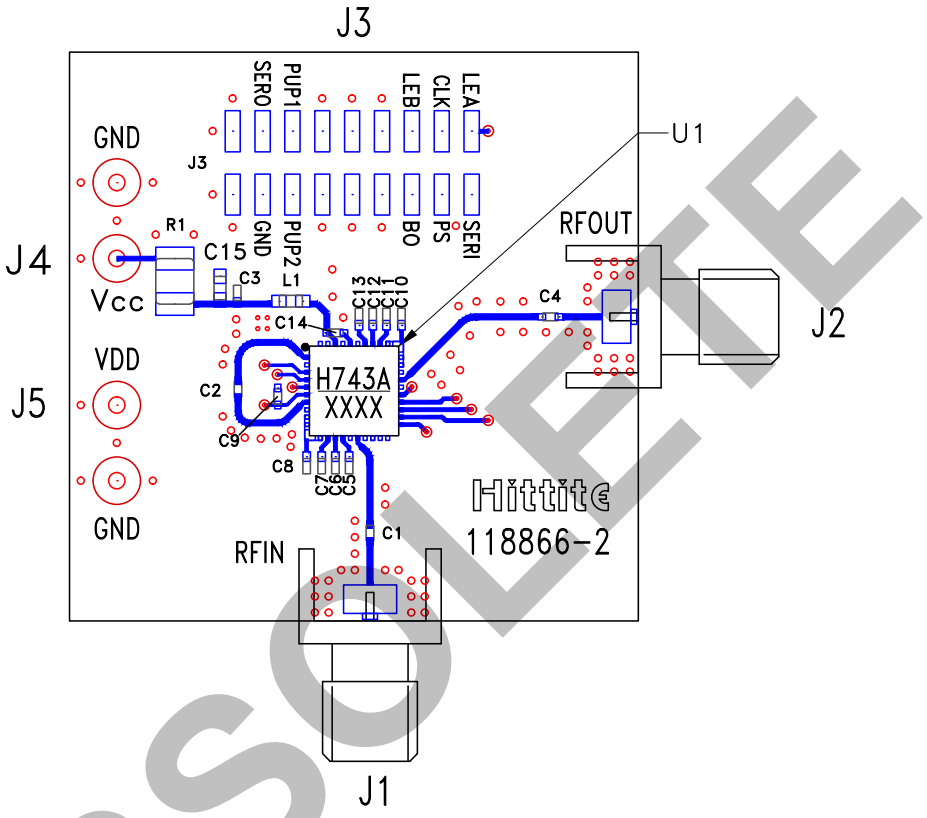
Evaluation PCB



List of Materials for Evaluation [1]

Item	Description
J1, J2	PCB Mount SMA Connector
J3	18 pos Header, 2mm
J4, J5	DC Pin
C1 - C4	Capacitor, 0402 Pkg. [1]
C5 - C7	330 pF Capacitor, 0402 Pkg.
C8, C10	Capacitor, 0402 Pkg. [1]
C9	100 pF Capacitor, 0402 Pkg.
C15	Capacitor, 0603 Pkg. [1]
L1	Inductor, 0603 Pkg.
R1	1.8 Ohm Resistor, 1206 Pkg.
U1	HMC743ALP6CE Variable Gain Amplifier
PCB [2]	118866 Evaluation PCB

[1] Please reference Components for Selected Frequencies Table

[2] Circuit Board Material: Arlon 25FR or Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

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